14-Bit, 160 MSPS TxDAC+® with 2× Interpolation Filter

AD9772A

FEATURES

Single 3.1 V to 3.5 V Supply
14-Bit DAC Resolution and Input Data Width
160 MSPS Input Data Rate
67.5 MHz Reconstruction Pass Band @ 160 MSPS
74 dBc SFDR @ 25 MHz
2× Interpolation Filter with High- or Low-Pass Response
73 dB Image Rejection with 0.005 dB Pass-band Ripple
Zero-Stuffing Option for Enhanced Direct IF Performance
Internal 2×/4× Clock Multiplier
250 mW Power Dissipation; 13 mW with Power-Down Mode
48-Lead LQFP Package

APPLICATIONS

Communication Transmit Channel
W-CDMA Base Stations, Multicarrier Base Stations, Direct IF Synthesis, Wideband Cable Systems
Instrumentation

GENERAL DESCRIPTION

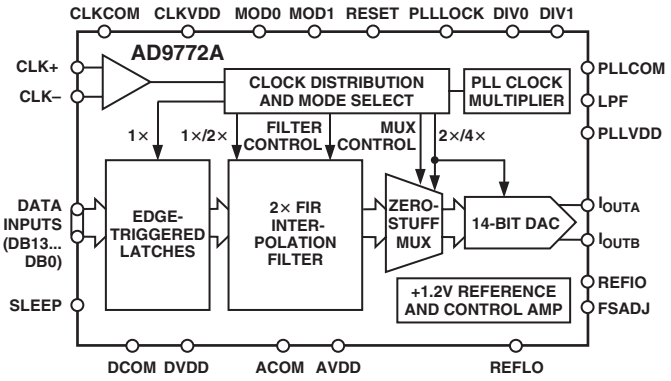
The AD9772A is a single-supply, oversampling, 14-bit digital-to-analog converter (DAC) optimized for baseband or IF waveform reconstruction applications requiring exceptional dynamic range. Manufactured on an advanced CMOS process, it integrates a complete, low distortion 14-bit DAC with a 2× digital interpolation filter and clock multiplier. The on-chip PLL clock multiplier provides all the necessary clocks for the digital filter and the 14-bit DAC. A flexible differential clock input allows for a single-ended or differential clock driver for optimum jitter performance.

For baseband applications, the 2× digital interpolation filter provides a low-pass response, thus providing as much as a threefold reduction in the complexity of the analog reconstruction filter. It does so by multiplying the input data rate by a factor of 2 while suppressing the original upper in-band image by more than 73 dB. For direct IF applications, the 2× digital interpolation filter response can be reconfigured to select the upper in-band image (i.e., high-pass response) while suppressing the original baseband image. To increase the signal level of the higher IF images and their pass-band flatness in direct IF applications, the AD9772A also features a zero-stuffing option in which the data following the 2× interpolation filter is upsampled by a factor of 2 by inserting midscale data samples.

The AD9772A can reconstruct full-scale waveforms with bandwidths as high as 67.5 MHz while operating at an input data rate of 160 MSPS. The 14-bit DAC provides differential current outputs to support differential or single-ended applications.

REV. B

FUNCTIONAL BLOCK DIAGRAM



A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The differential current outputs may be fed into a transformer or a differential op amp topology to obtain a single-ended output voltage using an appropriate resistive load.

The on-chip band gap reference and control amplifier are configured for maximum accuracy and flexibility. The AD9772A can be driven by the on-chip reference or by a variety of external reference voltages. The full-scale current of the AD9772A can be adjusted over a 2 mA to 20 mA range, thus providing additional gain ranging capabilities.

The AD9772A is available in a 48-lead LQFP package and is specified for operation over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. A flexible, low power 2× interpolation filter supporting reconstruction bandwidths of up to 67.5 MHz can be configured for a low- or high-pass response with 73 dB of image rejection for traditional baseband or direct IF applications.
2. A zero-stuffing option enhances direct IF applications.
3. A low glitch, fast settling 14-bit DAC provides exceptional dynamic range for both baseband and direct IF waveform reconstruction applications.
4. The AD9772A digital interface, consisting of edge-triggered latches and a flexible differential or single-ended clock input, can support input data rates up to 160 MSPS.
5. On-chip PLL clock multiplier generates all of the internal high speed clocks required by the interpolation filter and DAC.
6. The current output(s) of the AD9772A can easily be configured for various single-ended or differential circuit topologies.

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AD9772A–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)		±3.5		LSB
Differential Nonlinearity (DNL)		±2.0		LSB
Monotonicity (12-Bit)	Guaranteed over Specified Temperature Range			
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (without Internal Reference)	–2	±0.5	+2	% of FSR
Gain Error (with Internal Reference)	–5	±1.5	+5	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	–1.0		+1.25	V
Output Resistance		200		kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		1		μA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (REFLO = 3 V)		10		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift		0		ppm of FSR/°C
Gain Drift (without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (with Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
AVDD				
Voltage Range	3.1	3.3	3.5	V
Analog Supply Current (I_{AVDD})		34	37	mA
Analog Supply Current in SLEEP Mode (I_{AVDD})		4.3	6	mA
DVDD1, DVDD2				
Voltage Range	3.1	3.3	3.5	V
Digital Supply Current (I_{DVDD1} + I_{DVDD2})		37	40	mA
CLKVDD, PLLVDD[4] (PLLVDD = 3.3 V)				
Voltage Range	3.1	3.3	3.5	V
Clock Supply Current (I_{CLKVDD} + I_{PLLVDD})		25	30	mA
CLKVDD (PLLVDD = 0 V)				
Voltage Range	3.1	3.3	3.5	V
Clock Supply Current (I_{CLKVDD})		6.0		mA
Nominal Power Dissipation[5]		253	272	mW
Power Supply Rejection Ratio (PSRR)[6] – AVDD	–0.6		+0.6	% of FSR/V
Power Supply Rejection Ratio (PSRR)[6] – DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at I_{OUTA} driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.
[3]Use an external amplifier to drive any external load.
[4]Measured at f_{DATA} = 100 MSPS and f_{OUT} = 1 MHz, DIV1, DIV0 = 0 V.
[5]Measured with PLL enabled at f_{DATA} = 50 MSPS and f_{OUT} = 1 MHz.
[6]Measured over a 3.0 V to 3.6 V range.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, DVDD = 3.3 V, PLLVDD = 3.3 V, I_{OUTFS} = 20 mA, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum DAC Output Update Rate (f_{DAC})	400			MSPS
Output Settling Time (t_{ST}) (to 0.025%)		11		ns
Output Propagation Delay[1] (t_{PD})		17		ns
Output Rise Time (10% to 90%)[2]		0.8		ns
Output Fall Time (10% to 90%)[2]		0.8		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
AC LINEARITY—BASEBAND MODE				
Spurious-Free Dynamic Range (SFDR) to Nyquist (f_{OUT} = 0 dBFS)				
f_{DATA} = 65 MSPS; f_{OUT} = 1.01 MHz		82		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 10.01 MHz		75		dBc
f_{DATA} = 65 MSPS; f_{OUT} = 25.01 MHz		73		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 5.02 MHz		82		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 20.02 MHz		75		dBc
f_{DATA} = 160 MSPS; f_{OUT} = 50.02 MHz		65		dBc
Two-Tone Intermodulation (IMD) to Nyquist (f_{OUT1} = f_{OUT2} = –6 dBFS)				
f_{DATA} = 65 MSPS; f_{OUT1} = 5.01 MHz; f_{OUT2} = 6.01 MHz		85		dBc
f_{DATA} = 65 MSPS; f_{OUT1} = 15.01 MHz; f_{OUT2} = 17.51 MHz		75		dBc
f_{DATA} = 65 MSPS; f_{OUT1} = 24.1 MHz; f_{OUT2} = 26.2 MHz		68		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 10.02 MHz; f_{OUT2} = 12.02 MHz		85		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 30.02 MHz; f_{OUT2} = 35.02 MHz		70		dBc
f_{DATA} = 160 MSPS; f_{OUT1} = 48.2 MHz; f_{OUT2} = 52.4 MHz		65		dBc
Total Harmonic Distortion (THD)				
f_{DATA} = 65 MSPS; f_{OUT} = 1.0 MHz; 0 dBFS		–80		dB
f_{DATA} = 78 MSPS; f_{OUT} = 10.01 MHz; 0 dBFS		–74		dB
Signal-to-Noise Ratio (SNR)				
f_{DATA} = 65 MSPS; f_{OUT} = 16.26 MHz; 0 dBFS		71		dB
f_{DATA} = 100 MSPS; f_{OUT} = 25.1 MHz; 0 dBFS		71		dB
Adjacent Channel Power Ratio (ACPR)				
WCDMA with 4.1 MHz BW, 5 MHz Channel Spacing				
IF = 16 MHz, f_{DATA} = 65.536 MSPS		78		dBc
IF = 32 MHz, f_{DATA} = 131.072 MSPS		68		dBc
Four-Tone Intermodulation				
15.6 MHz, 15.8 MHz, 16.2 MHz, and 16.4 MHz at –12 dBFS		88		dBFS
f_{DATA} = 65 MSPS, Missing Center				
AC LINEARITY—IF MODE				
Four-Tone Intermodulation at IF = 70 MHz				
68.1 MHz, 69.3 MHz, 71.2 MHz, and 72.0 MHz at –20 dBFS		77		dBFS
f_{DATA} = 52 MSPS, f_{DAC} = 208 MHz				

NOTES
[1]Propagation delay is delay from CLK input to DAC update.
[2]Measured single-ended into 50Ω load.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current*	–10		+10	μA
Logic 0 Current	–10		+10	μA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
PLL CLOCK ENABLED—FIGURE 1a				
Input Setup Time (t_S), T_A = 25°C	0.5			ns
Input Hold Time (t_H), T_A = 25°C	1.0			ns
Latch Pulsewidth (t_{LPW}), T_A = 25°C	1.5			ns
PLL CLOCK DISABLED—FIGURE 1b				
Input Setup Time (t_S), T_A = 25°C	–1.2			ns
Input Hold Time (t_H), T_A = 25°C	3.2			ns
Latch Pulsewidth (t_{LPW}), T_A = 25°C	1.5			ns
CLK/PLLLOCK Delay (t_{OD}), T_A = 25°C	2.8		3.2	ns
PLLLOCK (V_{OH}), T_A = 25°C	3.0			V
PLLLOCK (V_{OL}), T_A = 25°C			0.3	V

*MOD0, MOD1, DIV0, DIV1, SLEEP, RESET have typical input currents of 15 μA.

Specifications subject to change without notice.

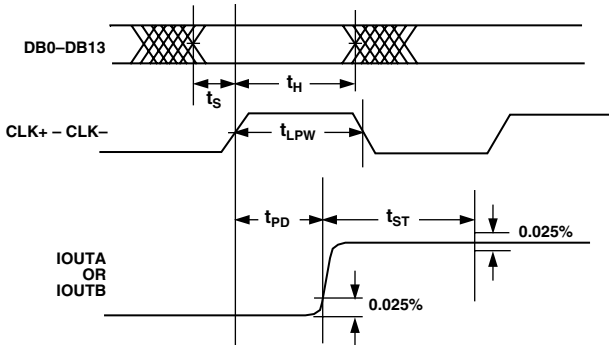


Figure 1a. Timing Diagram—PLL Clock Multiplier Enabled

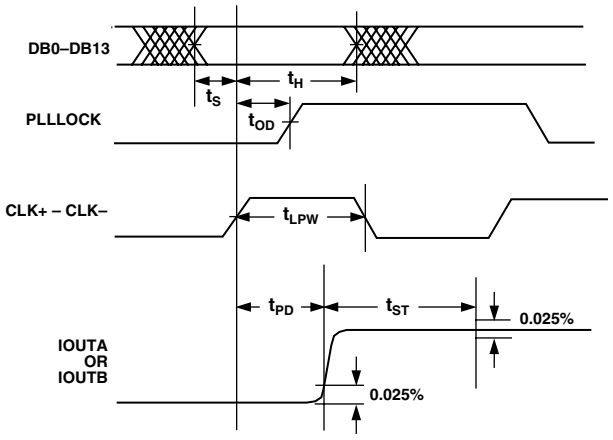


Figure 1b. Timing Diagram—PLL Clock Multiplier Disabled

DIGITAL FILTER SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, differential transformer-coupled output, 50 Ω doubly terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
MAXIMUM INPUT DATA RATE (f_{DATA})	150			MSPS
DIGITAL FILTER CHARACTERISTICS				
Pass-Bandwidth[1]: 0.005 dB		0.401		f_{OUT}/f_{DATA}
Pass-Bandwidth: 0.01 dB		0.404		f_{OUT}/f_{DATA}
Pass-Bandwidth: 0.1 dB		0.422		f_{OUT}/f_{DATA}
Pass-Bandwidth: –3 dB		0.479		f_{OUT}/f_{DATA}
LINEAR PHASE (FIR IMPLEMENTATION)				
STOP BAND REJECTION				
0.606 f_{CLOCK} to 1.394 f_{CLOCK}		73		dB
GROUP DELAY[2]		11		Input Clocks
IMPULSE RESPONSE DURATION				
–40 dB		36		Input Clocks
–60 dB		42		Input Clocks

NOTES
[1]Excludes sin(x)/x characteristic of DAC.
[2]Defined as the number of data clock cycles between impulse input and peak of output response.

Specifications subject to change without notice.

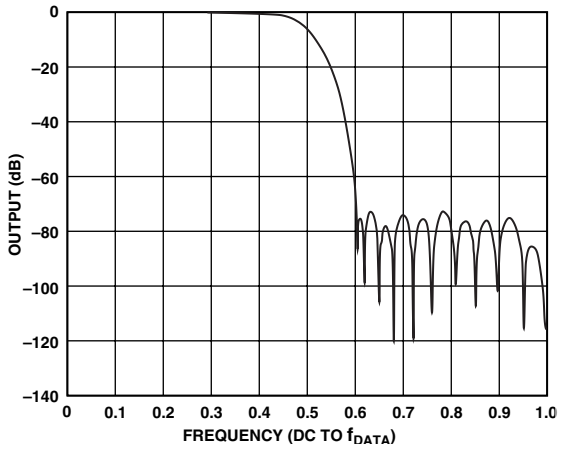


Figure 2a. FIR Filter Frequency Response—Baseband Mode

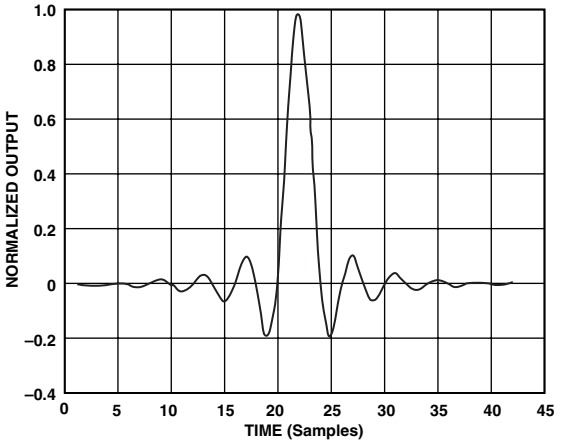


Figure 2b. FIR Filter Impulse Response—Baseband Mode

Table I. Integer Filter Coefficients for Interpolation Filter (43-Tap Half-Band FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(43)	10
H(2)	H(42)	0
H(3)	H(41)	–31
H(4)	H(40)	0
H(5)	H(39)	69
H(6)	H(38)	0
H(7)	H(37)	–138
H(8)	H(36)	0
H(9)	H(35)	248
H(10)	H(34)	0
H(11)	H(33)	–419
H(12)	H(32)	0
H(13)	H(31)	678
H(14)	H(30)	0
H(15)	H(29)	–1083
H(16)	H(28)	0
H(17)	H(27)	1776
H(18)	H(26)	0
H(19)	H(25)	–3282
H(20)	H(24)	0
H(21)	H(23)	10364
H(22)		16384

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD, DVDD1-2, CLKVDD, PLLVDD	ACOM, DCOM, CLKCOM, PLLCOM	–0.3	+4.0	V
AVDD, DVDD1-2, CLKVDD, PLLVDD	AVDD, DVDD1-2, CLKVDD, PLLVDD	–4.0	+4.0	V
ACOM, DCOM1-2, CLKCOM, PLLCOM	ACOM, DCOM1-2, CLKCOM, PLLCOM	–0.3	+0.3	V
REFIO, REFLO, FSADJ, SLEEP	ACOM	–0.3	AVDD + 0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–1.0	AVDD + 0.3	V
DB0–DB13, MOD0, MOD1, PLLLOCK	DCOM1-2	–0.3	DVDD + 0.3	V
CLK+, CLK–	CLKCOM	–0.3	CLKVDD + 0.3	V
DIV0, DIV1, RESET	CLKCOM	–0.3	CLKVDD + 0.3	V
LPF	PLLCOM	–0.3	PLLVDD + 0.3	V
Junction Temperature			125	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9772AAST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9772AASTRL	–40°C to +85°C	48-Lead LQFP	ST-48
AD9772A-EB		Evaluation Board	

*ST = Thin Plastic Quad Flatpack.

THERMAL CHARACTERISTIC

Thermal Resistance

48-Lead LQFP

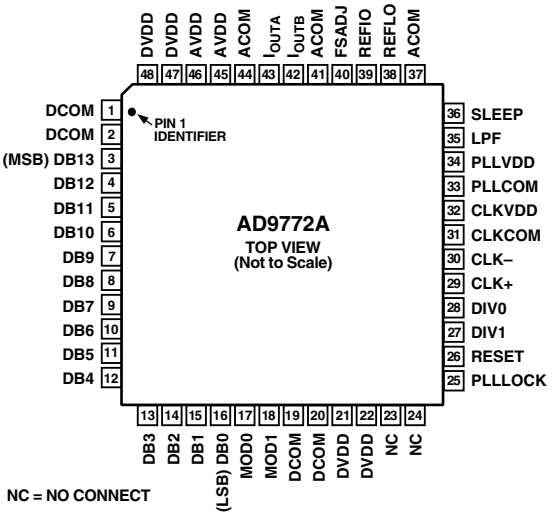
θ_{JA} = 91°C/W

θ_{JC} = 28°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9772A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1, 2, 19, 20	DCOM	Digital Common.
3	DB13	Most Significant Data Bit (MSB).
4–15	DB12–DB1	Data Bits 1–12.
16	DB0	Least Significant Data Bit (LSB).
17	MOD0	Invokes digital high-pass filter response (i. e., half-wave digital mixing mode). Active high.
18	MOD1	Invokes Zero-Stuffing Mode. Active high. Note, quarter-wave digital mixing occurs with MOD0 also set high.
23, 24	NC	No Connect, Leave Open.
21, 22, 47, 48	DVDD	Digital Supply Voltage (3.1 V to 3.5 V).
25	PLLLOCK	Phase-Lock Loop Lock Signal when PLL clock multiplier is enabled. High indicates PLL is locked to input clock. Provides 1× clock output when PLL clock multiplier is disabled. Maximum fanout is 1 (i.e., <10 pF).
26	RESET	Resets internal divider by bringing momentarily high when PLL is disabled to synchronize internal 1× clock to the input data and/or multiple AD9772A devices.
27, 28	DIV1, DIV0	DIV1 along with DIV0 sets the PLL's prescaler divide ratio (refer to Table III).
29	CLK+	Noninverting Input to Differential Clock. Bias to midsupply (i.e., CLKVDD/2).
30	CLK–	Inverting Input to Differential Clock. Bias to midsupply (i.e., CLKVDD/2).
31	CLKCOM	Clock Input Common.
32	CLKVDD	Clock Input Supply Voltage (3.1 V to 3.5 V).
33	PLLCOM	Phase-Lock Loop Common.
34	PLLVDD	Phase-Lock Loop (PLL) Supply Voltage (3.1 V to 3.5 V). To disable PLL clock multiplier, connect PLLVDD to PLLCOM.
35	LPF	PLL Loop Filter Node. This pin should be left as a no connect (open) unless the DAC update rate is less than 10 MSPS, in which case a series RC should be connected from LPF to PLLVDD as indicated on the evaluation board schematic.
36	SLEEP	Power-Down Control Input. Active high. Connect to ACOM if not used.
37, 41, 44	ACOM	Analog Common.
38	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
39	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., tie REFLO to ACOM). Requires 0.1 μF capacitor to ACOM when internal reference activated.
40	FSADJ	Full-Scale Current Output Adjust.
42	I_{OUTB}	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
43	I_{OUTA}	DAC Current Output. Full-scale current when all data bits are 1s.
45, 46	AVDD	Analog Supply Voltage (3.1 V to 3.5 V).

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s, minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

Signal-to-Noise Ratio (SNR)
S/N is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Pass Band
Frequency band in which any input applied therein passes unattenuated to the DAC output.

Stop-band Rejection
The amount of attenuation of a frequency outside the pass band applied to the DAC, relative to a full-scale signal applied at the DAC input within the pass band.

Group Delay
Number of input clocks between an impulse applied at the device input and peak DAC output current.

Impulse Response
Response of the device to an impulse applied to the input.

Adjacent Channel Power Ratio (ACPR)
A ratio in dBc between the measured power within a channel relative to its adjacent channel.

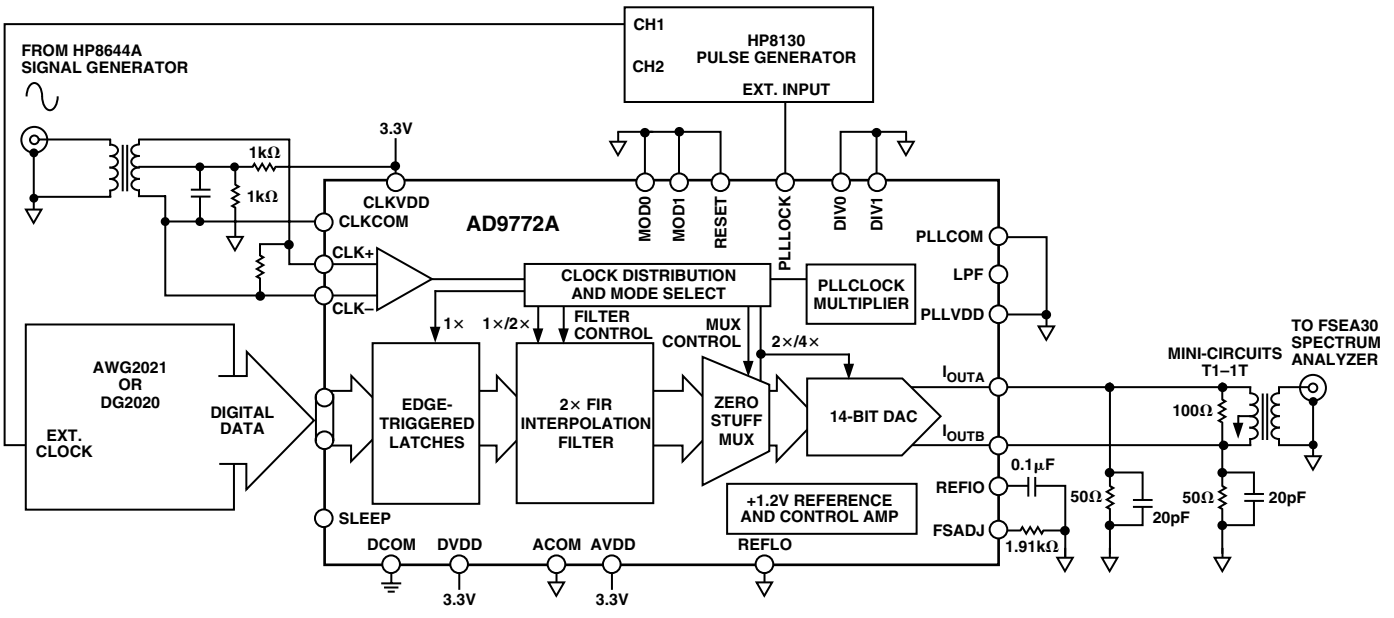
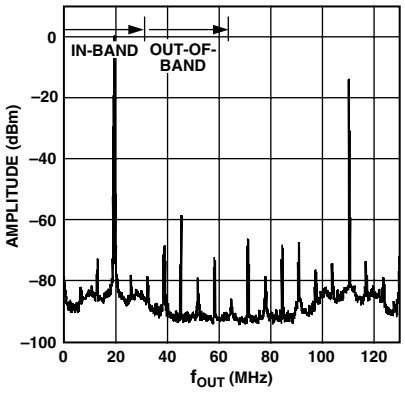
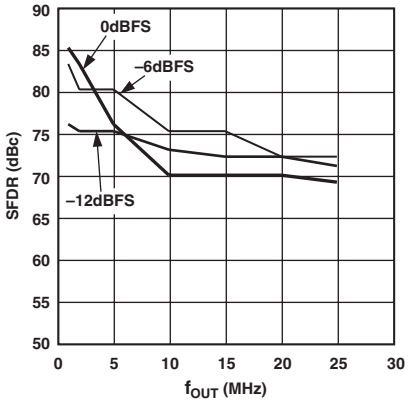


Figure 3. Basic AC Characterization Test Setup

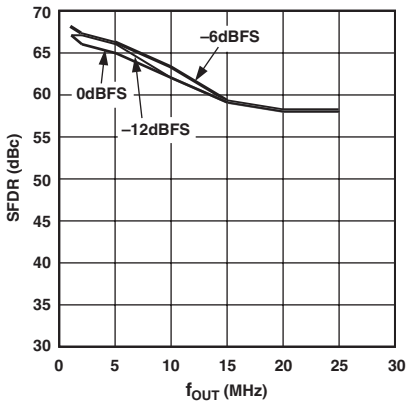
(AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA. PLL disabled.)



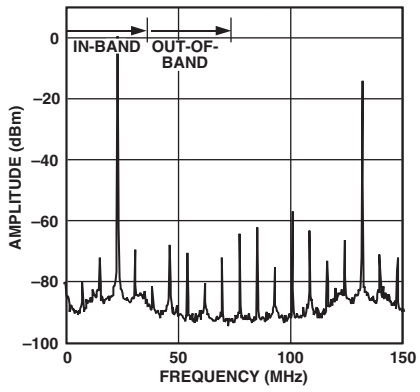
TPC 1. Single-Tone Spectral Plot @ f_{DATA} = 65 MSPS with $f_{OUT} = f_{DATA}/3$



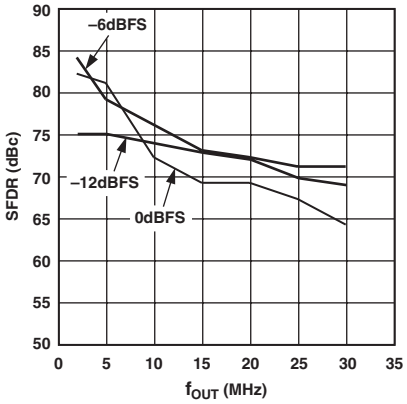
TPC 2. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS



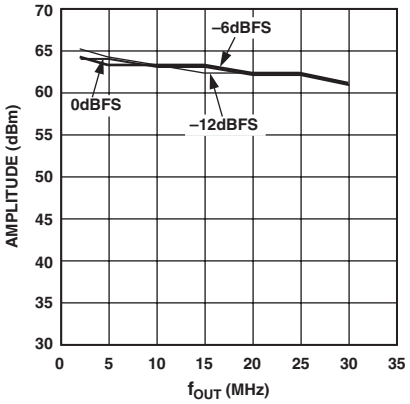
TPC 3. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 65 MSPS



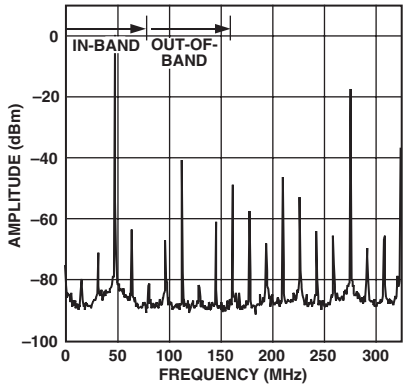
TPC 4. Single-Tone Spectral Plot @ f_{DATA} = 78 MSPS with $f_{OUT} = f_{DATA}/3$



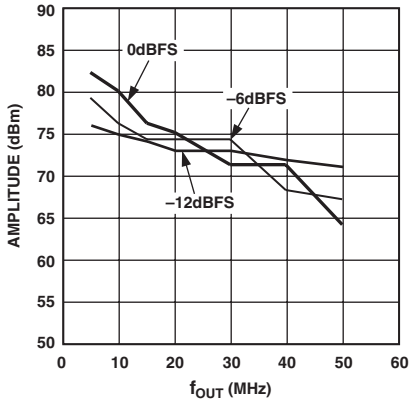
TPC 5. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS



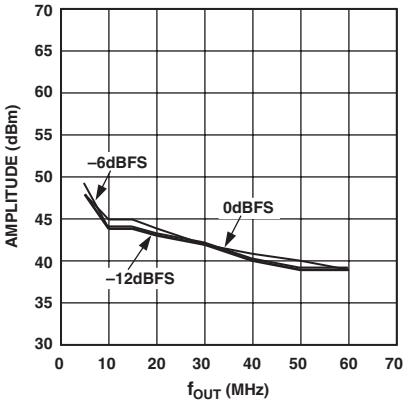
TPC 6. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 78 MSPS



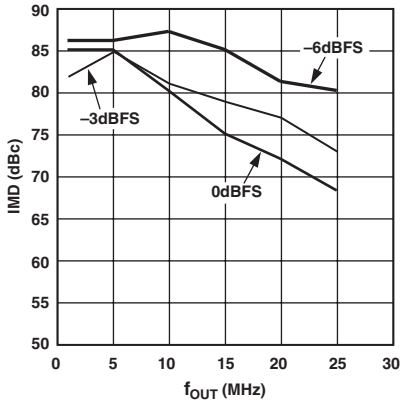
TPC 7. Single-Tone Spectral Plot @ f_{DATA} = 160 MSPS with $f_{OUT} = f_{DATA}/3$



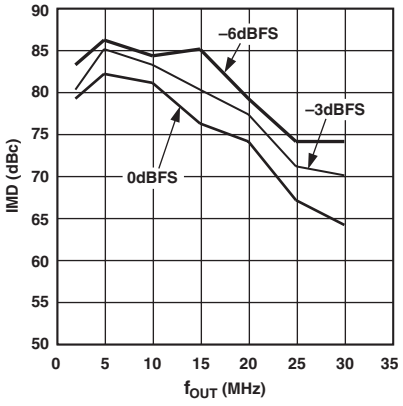
TPC 8. In-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS



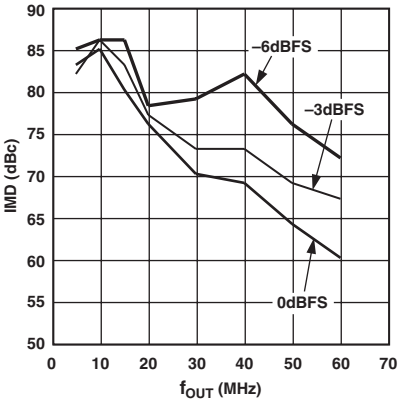
TPC 9. Out-of-Band SFDR vs. f_{OUT} @ f_{DATA} = 160 MSPS



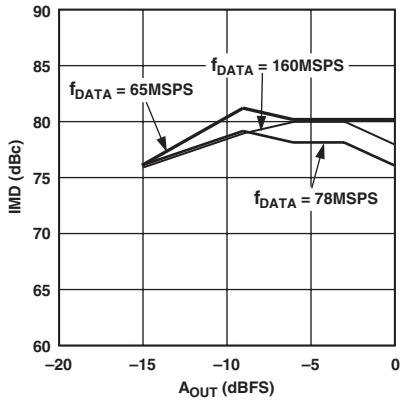
TPC 10. Third Order IMD Products vs. f_{OUT} @ f_{DATA} = 65 MSPS



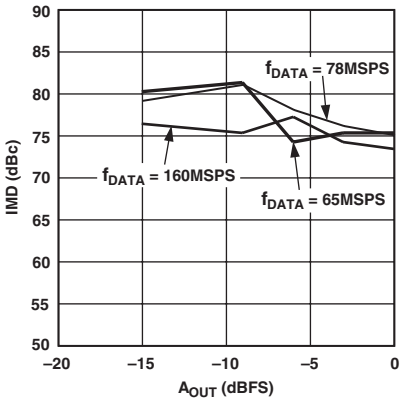
TPC 11. Third Order IMD Products vs. f_{OUT} @ f_{DATA} = 78 MSPS



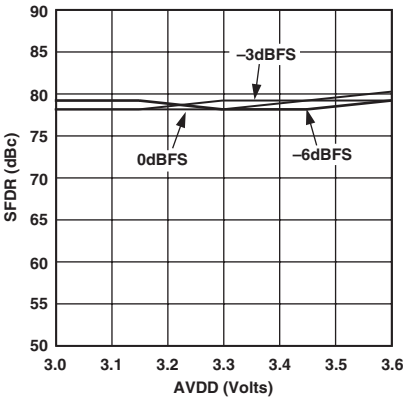
TPC 12. Third Order IMD Products vs. f_{OUT} @ f_{DATA} = 160 MSPS



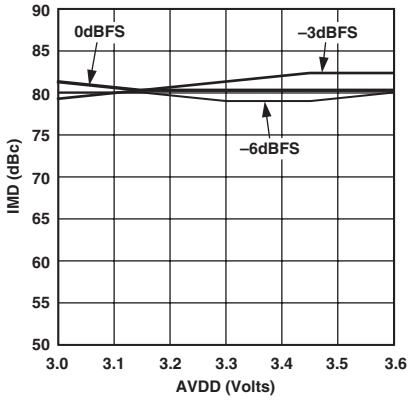
TPC 13. Third Order IMD Products vs. A_{OUT} @ f_{OUT} = f_{DAC}/11



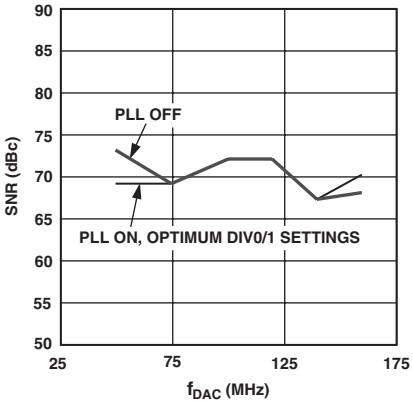
TPC 14. Third Order IMD Products vs. A_{OUT} @ f_{OUT} = f_{DAC}/5



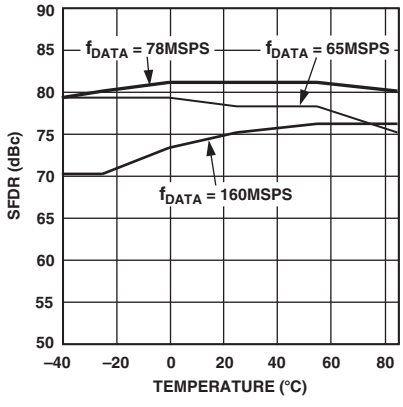
TPC 15. SFDR vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS



TPC 16. Third Order IMD Products vs. AVDD @ f_{OUT} = 10 MHz, f_{DAC} = 320 MSPS



TPC 17. SNR vs. f_{DAC} @ f_{OUT} = 10 MHz



TPC 18. In-Band SFDR vs. Temperature @ f_{OUT} = f_{DATA}/11

FUNCTIONAL DESCRIPTION

Figure 4 shows a simplified block diagram of the AD9772A. The AD9772A is a complete, 2× oversampling, 14-bit DAC that includes a 2× interpolation filter, a phase-locked loop (PLL) clock multiplier, and a 1.20 V band gap voltage reference. While the AD9772A's digital interface can support input data rates as high as 160 MSPS, its internal DAC can operate up to 400 MSPS, thus providing direct IF conversion capabilities. The 14-bit DAC provides two complementary current outputs whose full-scale current is determined by an external resistor. The AD9772A features a flexible, low jitter, differential clock input, providing excellent noise rejection while accepting a sine wave input. An on-chip PLL clock multiplier produces all of the necessary synchronized clocks from an external reference clock source. Separate supply inputs are provided for each functional block to ensure optimum noise and distortion performance. A SLEEP mode is also included for power savings.

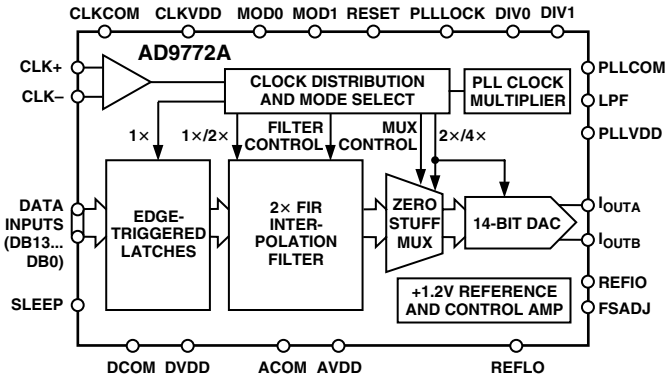


Figure 4. Functional Block Diagram

Preceding the 14-bit DAC is a 2× digital interpolation filter that can be configured for a low-pass (i.e., baseband mode) or high-pass (i.e., direct IF mode) response. The input data is latched into the edge-triggered input latches on the rising edge of the differential input clock as shown in Figure 1a and then interpolated by a factor of 2 by the digital filter. For traditional baseband applications, the 2× interpolation filter has a low-pass response. For direct IF applications, the filter's response can be converted into a high-pass response to extract the higher image. The output data of the 2× interpolation filter can update the 14-bit DAC directly or undergo a zero-stuffing process to increase the DAC update rate by another factor of 2. This action enhances the relative signal level and pass-band flatness of the higher images.

DIGITAL MODES OF OPERATION

The AD9772A features four different digital modes of operation controlled by the digital inputs, MOD0 and MOD1. MOD0 controls the 2× digital filter's response (i.e., low-pass or high-pass), while MOD1 controls the zero-stuffing option. The selected mode as shown in Table II will depend on whether the application requires the reconstruction of a baseband or IF signal.

Table II. Digital Modes

Digital Mode	MOD0	MOD1	Digital Filter	Zero-Stuffing
Baseband	0	0	Low	No
Baseband	0	1	Low	Yes
Direct IF	1	0	High	No
Direct IF	1	1	High	Yes

Applications requiring the highest dynamic range over a wide bandwidth should consider operating the AD9772A in a baseband mode. Note, the zero-stuffing option can also be used in this mode, however, the ratio of signal to image power will be reduced. Applications requiring the synthesis of IF signals should consider operating the AD9772A in a Direct IF mode. In this case, the zero-stuffing option should be considered when synthesizing and selecting IFs beyond the input data rate, f_{DATA}. If the reconstructed IF falls below f_{DATA}, the zero-stuffing option may or may not be beneficial. Note, the dynamic range (i.e., SNR/SFDR) is also optimized by disabling the PLL clock multiplier (i.e., PLLVDD to PLLCOM) and by using an external low jitter clock source operating at the DAC update rate, f_{DAC}.

2× Interpolation Filter Description

The 2× interpolation filter is based on a 43-tap half-band symmetric FIR topology that can be configured for a low- or high-pass response, depending on the state of the MOD0 control input. The low-pass response is selected with MOD0 low while the high-pass response is selected with MOD0 high. The low-pass frequency and impulse response of the half-band interpolation filter are shown in Figures 2a and 2b, while Table I lists the idealized filter coefficients. Note that a FIR filter's impulse response is also represented by its idealized filter coefficients.

The 2× interpolation filter essentially multiplies the input data rate to the DAC by a factor of 2, relative to its original input data rate, while reducing the magnitude of the first image associated with the original input data rate occurring at $f_{DATA} - f_{FUNDAMENTAL}$. Note, as a result of the 2× interpolation, the digital filter's frequency response is uniquely defined over its Nyquist zone of dc to f_{DATA}, with mirror images occurring in adjacent Nyquist zones.

The benefits of an interpolation filter are clearly seen in Figure 5, which shows an example of the frequency and time domain representation of a discrete time sine wave signal before and after it is applied to the 2× digital interpolation filter in a low-pass configuration. Images of the sine wave signal appear around multiples of the DAC's input data rate (i.e., f_{DATA}) as predicted by sampling theory. These undesirable images will also appear at the output of a reconstruction DAC, although attenuated by the DAC's sin(x)/x roll-off response.

In many band-limited applications, the images from the reconstruction process must be suppressed by an analog filter following the DAC. The complexity of this analog filter is typically determined by the proximity of the desired fundamental to the first image and the required amount of image suppression. Adding to the complexity of this analog filter may be the requirement of compensating for the DAC's sin(x)/x response.

Referring to Figure 5, the new first image associated with the DAC's higher data rate after interpolation is pushed out further relative to the input signal, since it now occurs at 2× $f_{DATA} - f_{FUNDAMENTAL}$. The old first image associated with the lower DAC data rate before interpolation is suppressed by the digital filter. As a result, the transition band for the analog reconstruction filter is increased, thus reducing the complexity of the analog filter. Furthermore, the sin(x)/x roll-off over the original input data pass band (i.e., dc to $f_{DATA}/2$) is significantly reduced.

As previously mentioned, the 2× interpolation filter can be converted into a high-pass response, thus suppressing the fundamental while passing the original first image occurring at $f_{DATA} - f_{FUNDAMENTAL}$. Figure 6 shows the time and frequency representation for a high-pass response of a discrete time sine wave. This action can also be modeled as a 1/2 wave digital mixing process in which the impulse response of the low-pass filter is digitally mixed with a square wave having a frequency of exactly $f_{DATA}/2$. Since the even coefficients have a zero value (refer to Table I), this process simplifies into inverting the center coefficient of the low-pass filter (i.e., invert H(18)). Note that this also corresponds to inverting the peak of the impulse response shown in Figure 2a. The resulting high-pass frequency response becomes the frequency inverted mirror image of the low-pass filter response shown in Figure 2b.

It is worth noting that the new first image now occurs at $f_{DATA} + f_{FUNDAMENTAL}$. A reduced transition region of $2 \times f_{FUNDAMENTAL}$ exists for image selection, thus mandating that the $f_{FUNDAMENTAL}$ be placed sufficiently high for practical filtering purposes in direct IF applications. Also, the lower side-band images occurring at $f_{DATA} - f_{FUNDAMENTAL}$ and its multiples (i.e., $N \times f_{DATA} - f_{FUNDAMENTAL}$) experience a frequency inversion while the upper sideband images occurring at $f_{DATA} + f_{FUNDAMENTAL}$ and its multiples (i.e., $N \times f_{DATA} + f_{FUNDAMENTAL}$) do not.

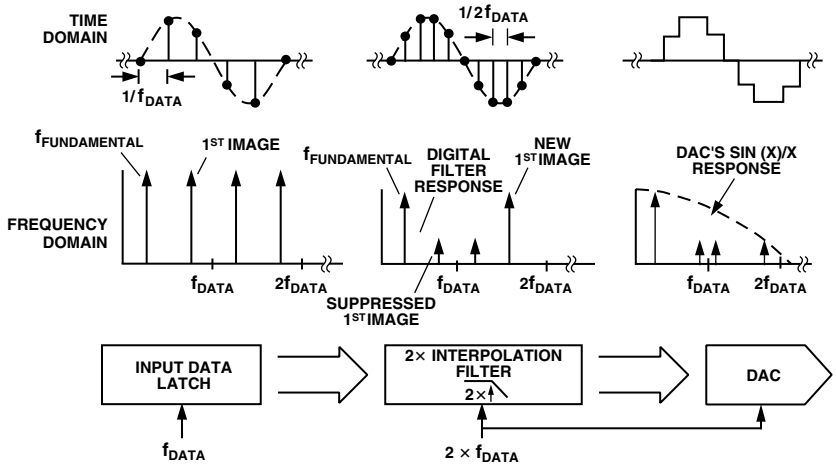


Figure 5. Time and Frequency Domain Example of Low-Pass 2× Digital Interpolation Filter

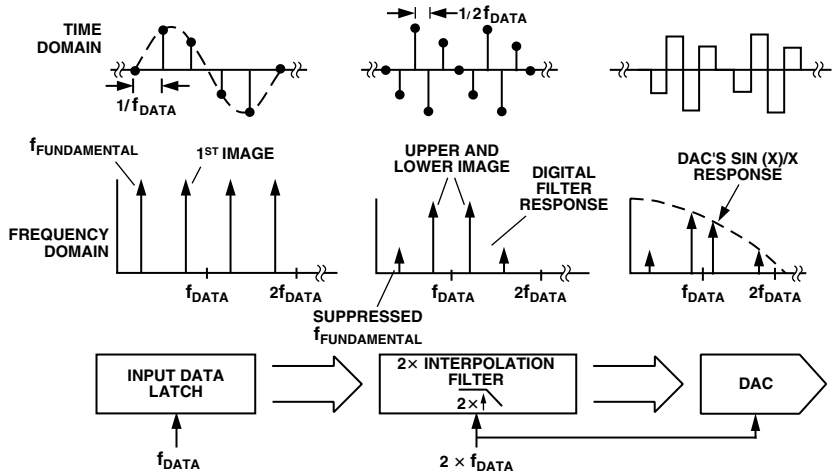


Figure 6. Time and Frequency Domain Example of High-Pass 2× Digital Interpolation Filter

Zero-Stuffing Option Description

As shown in Figure 7, a zero or null in the frequency responses (after interpolation and DAC reconstruction) occurs at the final DAC update rate (i.e., 2× f_{DATA}) due to the DAC's inherent sin(x)/x roll-off response. In baseband applications, this roll-off in the frequency response may not be as problematic since much of the desired signal energy remains below $f_{DATA}/2$ and the amplitude variation is not as severe. However, in direct IF applications interested in extracting an image above $f_{DATA}/2$, this roll-off may be problematic due to the increased pass-band amplitude variation as well as the reduced signal level of the higher images.

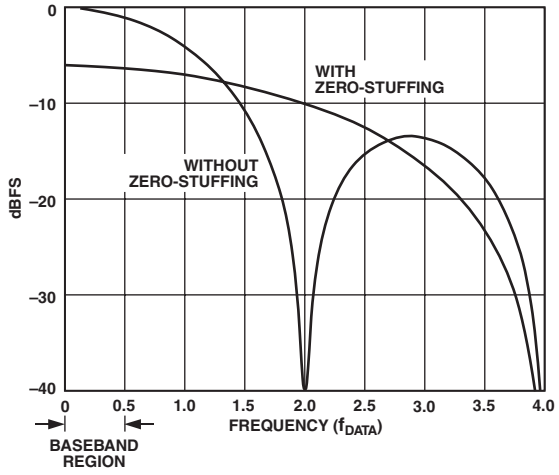


Figure 7. Effects of Zero-Stuffing on DAC's Sin(x)/x Response

For instance, if the digital data into the AD9772A represented a baseband signal centered around $f_{DATA}/4$ with a pass band of $f_{DATA}/10$, the reconstructed baseband signal out of the AD9772A would experience only a 0.18 dB amplitude variation over its pass band with the first image occurring at 7/4 f_{DATA} with 17 dB of attenuation relative to the fundamental. However, if the high-pass filter response was selected, the AD9772A would now produce pairs of images at $[(2N + 1) \times f_{DATA}] \pm f_{DATA}/4$ where N = 0, 1. . . Note, due to the DAC's sin(x)/x response, only the lower or upper side-band images centered around f_{DATA} may be useful, although they would be attenuated by –2.1 dB and –6.54 dB, respectively, as well as experience a pass-band amplitude roll-off of 0.6 dB and 1.3 dB.

To improve upon the pass-band flatness of the desired image and/or to extract higher images (i.e., $3 \times f_{DATA} \pm f_{FUNDAMENTAL}$) the zero-stuffing option should be employed by bringing the MOD1 pin high. This option increases the effective DAC update rate by another factor of 2 since a midscale sample (i.e., 10 0000 0000 0000) is inserted after every data sample originating from the 2× interpolation filter. A digital multiplexer switching at a rate of $4 \times f_{DATA}$ between the interpolation filter's output and a data register containing the midscale data sample is used to implement this option as shown in Figure 6. Therefore, the DAC output is now forced to return to its differential midscale current value (i.e., $I_{OUTA} - I_{OUTB}$ @ 0 mA) after reconstructing each data sample from the digital filter.

The net effect is to increase the DAC update rate such that the zero in the sin(x)/x frequency response now occurs at $4 \times f_{DATA}$ along with a corresponding reduction in output power as shown in Figure 7. Note that if the 2× interpolation filter's high-pass response is also selected, this action can be modeled as a 1/4 wave digital mixing process, since this is equivalent to digitally mixing the impulse response of the low-pass filter with a square wave having a frequency of exactly f_{DATA} (i.e., $f_{DAC}/4$).

It is important to realize that the zero-stuffing option by itself does not change the location of the images but rather their signal level, amplitude flatness, and relative weighting. For instance, in the previous example, the pass-band amplitude flatness of the lower and upper side-band images centered around f_{DATA} are improved to 0.14 dB and 0.24 dB, respectively, while the signal level has changed to –6.5 dBFS and –7.5 dBFS. The lower or upper side-band image centered around $3 \times f_{DATA}$ will exhibit an amplitude flatness of 0.77 dB and 1.29 dB with signal levels of approximately –14.3 dBFS and –19.2 dBFS.

PLL CLOCK MULTIPLIER OPERATION

The phase-lock loop (PLL) clock multiplier circuitry, along with the clock distribution circuitry, can produce the necessary internally synchronized 1×, 2×, and 4× clocks for the edge triggered latches, 2× interpolation filter, zero-stuffing multiplier, and DAC. Figure 8 shows a functional block diagram of the PLL clock multiplier, which consists of a phase detector, a charge pump, a voltage controlled oscillator (VCO), a prescaler, and digital control inputs/outputs. The clock distribution circuitry generates all the internal clocks for a given mode of operation. The charge pump and VCO are powered from PLLVDD, while the differential clock input buffer, phase detector, prescaler, and clock distribution circuitry are powered from CLKVDD. To ensure optimum phase noise performance from the PLL clock multiplier and clock distribution circuitry, PLLVDD and CLKVDD must originate from the same clean analog supply.

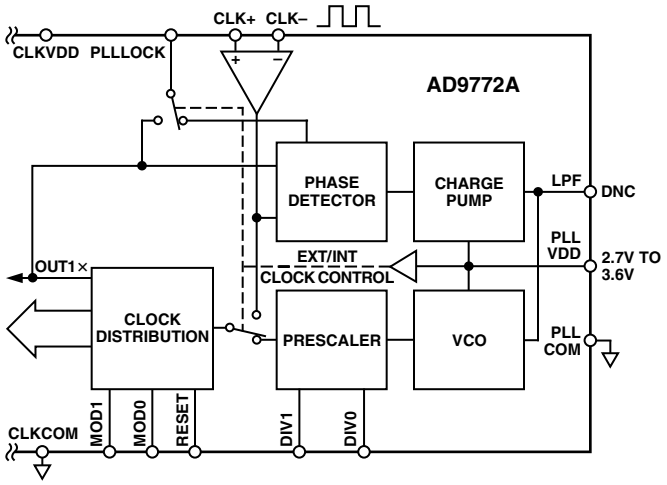


Figure 8. Clock Multiplier with PLL Clock Multiplier Enabled

The PLL clock multiplier has two modes of operation. It can be enabled for less demanding applications, providing a reference clock meeting the minimum specified input data rate of 6 MSPS. It can be disabled for applications below this data rate or for applications requiring higher phase noise performance. In this case, a reference clock at twice the input data rate (i.e., $2 \times f_{DATA}$) must be provided without the zero-stuffing option selected and four

times the input data rate (i.e., 4 × f_{DATA}) with the zero-stuffing option selected. Note, multiple AD9772A devices can be synchronized in either mode if driven by the same reference clock, since the PLL clock multiplier when enabled ensures synchronization. RESET can be used for synchronization if the PLL clock multiplier is disabled.

Figure 8 shows the proper configuration used to enable the PLL clock multiplier. In this case, the external clock source is applied to CLK+ (and/or CLK–) and the PLL clock multiplier is fully enabled by connecting PLLVDD to CLKVDD.

The settling/acquisition time characteristics of the PLL are also dependent on the divide-by-N ratio as well as the input data rate. In general, the acquisition time increases with increasing data rate (for fixed divide-by-N ratio) or increasing divide-by-N ratio (for fixed input data rate).

Since the VCO can operate over a 96 MHz to 400 MHz range, the prescaler divide-by-ratio following the VCO must be set according to Table III for a given input data rate (i.e., f_{DATA}) to ensure optimum phase noise and successful locking. In general, the best phase noise performance for any prescaler setting is achieved with the VCO operating near its maximum output frequency of 400 MHz. Note, the divide-by-N ratio also depends on whether the zero-stuffing option is enabled since this option requires the DAC to operate at 4× the input data rate. The divide-by-N ratio is set by DIV1 and DIV0.

With the PLL clock multiplier enabled, PLLLOCK serves as an active high control output that may be monitored upon system power-up to indicate that the PLL is successfully locked to the input clock. Note, when the PLL clock multiplier is not locked, PLLLOCK will toggle between logic high and low in an asynchronous manner until locking is finally achieved. As a result, it is recommended that PLLLOCK, if monitored, be sampled several times to detect proper locking 100 ms after power-up.

Table III. Recommended Prescaler Divide-by-N Ratio Settings

f_{DATA} (MSPS)	MOD1	DIV1	DIV0	Divide-by-N Ratio
48–160	0	0	0	1
24–100	0	0	1	2
12–50	0	1	0	4
6–25	0	1	1	8
24–100	1	0	0	1
12–50	1	0	1	2
6–25	1	1	0	4
3–12.5	1	1	1	8

As stated earlier, applications requiring input data rates below 6 MSPS must disable the PLL clock multiplier and provide an external reference clock. However, applications already containing a low phase noise (i.e., jitter) reference clock that is twice (or four times) the input data rate should consider disabling the PLL clock multiplier to achieve the best SNR performance from the AD9772A. Note that the SFDR performance and wideband noise performance of the AD9772A remain unaffected with or without the PLL clock multiplier enabled.

The effects of phase noise on the AD9772A's SNR performance become more noticeable at higher reconstructed output frequencies and signal levels. Figure 9 compares the phase noise of a full-scale sine wave at exactly $f_{DATA}/4$ at different data rates (therefore carrier frequency) with the optimum DIV1, DIV0 setting. The effects of phase noise, and its effect on a signal's CNR performance, become even more evident at higher IF frequencies as shown in Figure 10. In both instances, it is the narrow-band phase noise that limits the CNR performance.

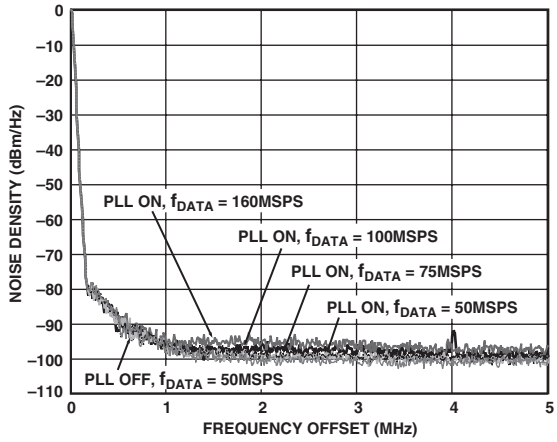


Figure 9. Phase Noise of PLL Clock Multiplier at Exact $f_{OUT} = f_{DATA}/4$ at Different f_{DATA} Settings with Optimum DIV0/DIV1 Settings Using R & S FSEA30, RBW = 30 kHz

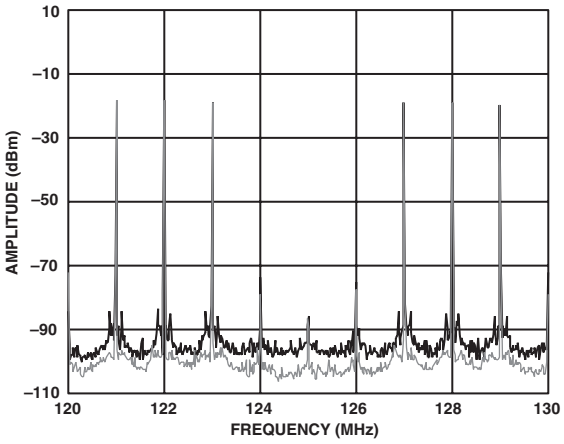


Figure 10. Direct IF Mode Reveals Phase Noise Degradation with and without PLL Clock Multiplier (IF = 125 MHz and f_{DATA} = 100 MSPS)

To disable the PLL clock multiplier, connect PLLVDD to PLLCOM as shown in Figure 11. LPF may remain open since this portion of the PLL circuitry is now disabled. The differential clock input should be driven with a reference clock twice the data input rate in baseband applications and four times the data input rate in direct IF applications in which the 1/4 wave mixing option is employed (i.e., MOD1 and MOD0 active high). The clock distribution circuitry remains enabled providing a 1× internal clock at PLLLOCK. Digital input data is latched into the AD9772 on every other rising edge of the differential clock input. The rising

edge that corresponds to the input latch immediately precedes the rising edge of the 1× clock at PLLLOCK. Adequate setup and hold time for the input data as shown in Figure 1b should be allowed. Note that enough delay is present between CLK+/CLK– and the data input latch to cause the minimum setup time for input data to be negative. This is noted in the Digital Specifications section. PLLLOCK contains a relatively weak driver output, with its output delay (t_{OD}) sensitive to output capacitance loading. Thus PLLLOCK should be buffered for fanouts greater than 1, and/or load capacitance greater than 10 pF. If a data timing issue exists between the AD9772A and its external driver device, the 1× clock appearing at PLLLOCK can be inverted via an external gate to ensure proper setup and hold time.

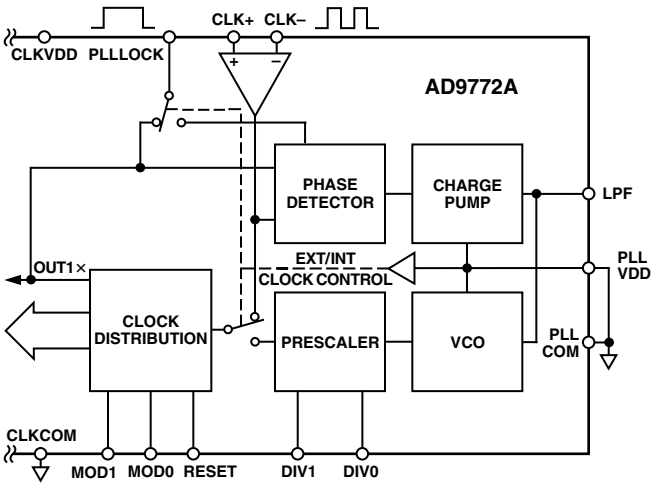


Figure 11. Clock Multiplier with PLL Clock Multiplier Disabled

SYNCHRONIZATION OF CLK/DATA USING RESET WITH PLL DISABLED

The relationship between the internal and external clocks in this mode is shown in Figure 12. A clock at the output update data rate (2× the input data rate) must be applied to the CLK inputs. Internal dividers create the internal 1× clock necessary for the input latches. With the PLL disabled, a delayed version of the 1× clock is present at the PLLLOCK pin. The DAC latch is updated on the particular rising edge of the external 2× clock, which corresponds to the rising edge of the 1× clock. Updates to the input data should be synchronized to this specific rising edge as shown in Figure 12. To ensure this synchronization, a Logic 1 should be momentarily applied to the RESET pin on power-up, before CLK is applied. Applying a momentary Logic 1 to RESET brings the 1× clock at PLLLOCK to a Logic 1. On the next rising edge of the 2× clock, the 1× clock will go to Logic 0. The following rising edge of the 2× clock will cause the 1× clock to go to Logic 1 again, as well as update the data in both of the input latches.

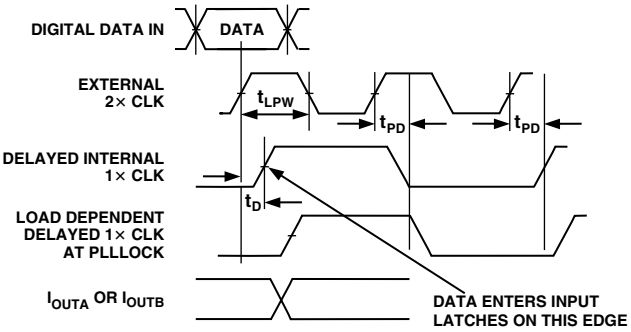


Figure 12. Internal Timing of AD9772A with PLL Disabled

Figures 13a and 13b illustrate the details of the RESET function timing. RESET going from a high to a low logic level enables the 1× clock output, generated by the PLLLOCK pin. If RESET goes low at a time well before the rising edge of the 2× clock as shown in Figure 13a, then PLLLOCK will go high on the following edge of the 2× clock. If RESET goes from a high to a low logic level 600 ps or later following the rising edge of the 2× clock as shown in Figure 13b, there will be a delay of one 2× clock cycle before PLLLOCK goes high. In either case, as long as RESET remains low, PLLLOCK will change state on every rising edge of the 2× clock. As stated before, it is the rising edge of the 2× clock that immediately precedes the rising edge of PLLLOCK that latches data into the AD9772A input latches.

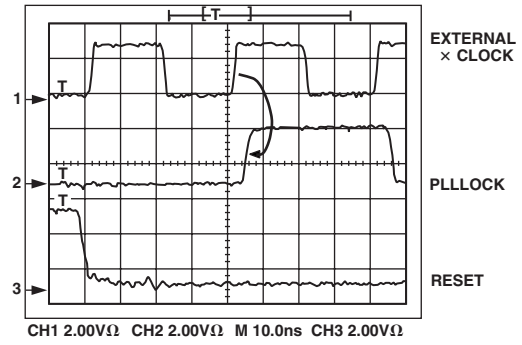


Figure 13a. RESET Timing with PLL Disabled

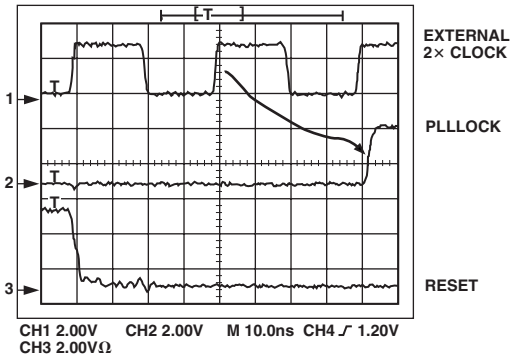


Figure 13b. RESET Timing with PLL Disabled and Insufficient Set-Up Time

DAC OPERATION

The 14-bit DAC along with the 1.2 V reference and reference control amplifier is shown in Figure 14. The DAC consists of a large PMOS current source array capable of providing up to 20 mA of full-scale current, I_{OUTFS}. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose values are 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits' current sources. All of these current sources are switched to one or the other of two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance.

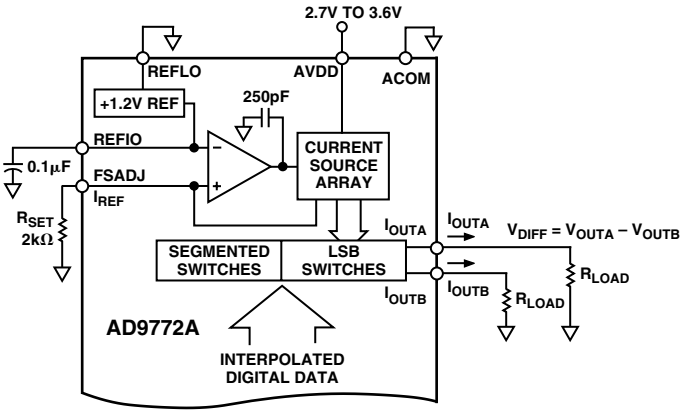


Figure 14. Block Diagram of Internal DAC, 1.2 V Reference, and Reference Control Circuits

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, as shown in Figure 14. R_{SET}, in combination with both the reference control amplifier and voltage reference, REFIO, sets the reference current, I_{REF}, which is mirrored to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is exactly 32 times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9772A provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as

$$I_{OUTA} = \left(DAC\ CODE/16384\right) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = \left(16383 - DAC\ CODE\right)/16384 \times I_{OUTFS} \quad (2)$$

where DAC CODE = 0 to 16383 (i.e., decimal representation).

As previously mentioned, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO}, and external resistor, R_{SET}. It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where:

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note that R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range of 1.25 V to prevent signal compression. To maintain optimum distortion and linearity performance, the maximum voltages at V_{OUTA} and V_{OUTB} should not exceed ±500 mV p-p.

The differential voltage, V_{DIFF}, appearing across I_{OUTA} and I_{OUTB}, is

$$V_{DIFF} = \left(I_{OUTA} - I_{OUTB}\right) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}; V_{DIFF} can be expressed as

$$V_{DIFF} = \left[\left(2\ DAC\ CODE - 16383\right)/16384\right] \times \left(32\ R_{LOAD}/R_{SET}\right) \times V_{REFIO} \quad (8)$$

The last two equations highlight some of the advantages of operating the AD9772A differentially. First, the differential operation will help cancel common-mode error sources such as noise, distortion, and dc offsets associated with I_{OUTA} and I_{OUTB}. Second, the differential code-dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9772A can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

REFERENCE OPERATION

The AD9772A contains an internal 1.20 V band gap reference that can easily be disabled and overridden by an external reference. REFIO serves as either an *output* or *input*, depending on whether the internal or external reference is selected. If REFLO is tied to ACOM, as shown in Figure 15, the internal reference is activated, and REFIO provides a 1.20 V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. If any additional loading is required, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA.

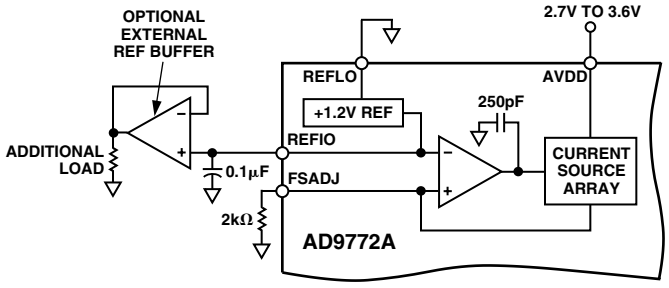


Figure 15. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external 1.2 V reference such as the AD1580 may then be applied to REFIO as shown in Figure 16. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled, and the high input impedance of REFIO minimizes any loading of the external reference.

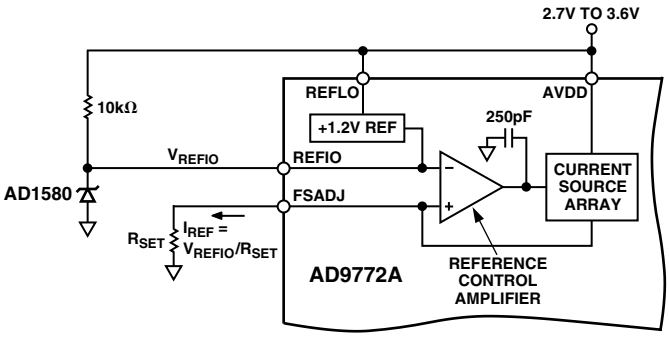


Figure 16. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9772A also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 16, such that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9772's DAC, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

I_{REF} can be controlled using the single-supply circuit shown in Figure 17 for a fixed R_{SET}. In this example, the internal reference is disabled, and the voltage of REFIO is varied over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply DAC or digital potentiometer, thus allowing I_{REF} to be digitally controlled for a fixed R_{SET}. This particular example shows the AD5220, an 8-bit serial input digital potentiometer, along with the AD1580 voltage reference. Note, since the input impedance of REFIO does interact and load the digital potentiometer wiper to create a slight nonlinearity in the programmable voltage divider ratio, a digital potentiometer with 10 kΩ or less resistance is recommended.

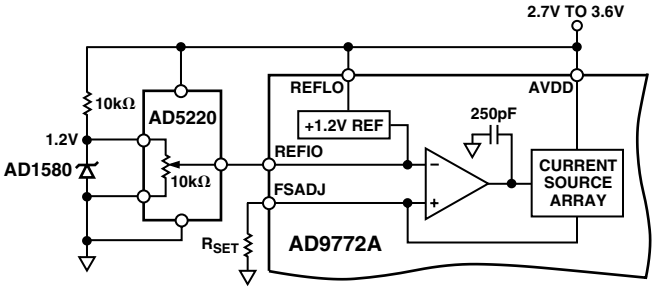


Figure 17. Single-Supply Gain Control Circuit

ANALOG OUTPUTS

The AD9772A produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section, by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 18 shows the equivalent analog output circuit of the AD9772A, which consists of a parallel combination of PMOS differential current switches associated with each segmented current source. The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches and is typically 200 kΩ in parallel with 3 pF. Due to the nature of a PMOS device, the output impedance is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) and, to a lesser extent, the analog supply voltage, AVDD, and full-scale current, I_{OUTFS}. Although the output impedance's signal dependency can be a source of dc nonlinearity and ac linearity (i.e., distortion), its effects can be limited if certain precautions are noted.

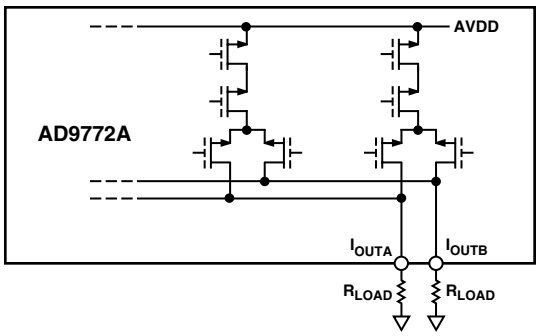


Figure 18. Equivalent Analog Output Circuit

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9772A. The positive output compliance range is

slightly dependent on the full-scale output current, I_{OUTFS}. Operation beyond the positive compliance range will induce clipping of the output signal, which severely degrades the AD9772A's linearity and distortion performance.

Operating the AD9772A with reduced voltage output swings at I_{OUTA} and I_{OUTB} in a differential or single-ended output configuration reduces the signal dependency of its output impedance, thus enhancing distortion performance. Although the voltage compliance range of I_{OUTA} and I_{OUTB} extends from –1.0 V to +1.25 V, optimum distortion performance is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed approximately 0.5 V. A properly selected transformer with a grounded center tap will allow the AD9772A to provide the required power and voltage levels to different loads while maintaining reduced voltage swings at I_{OUTA} and I_{OUTB}. DC-coupled applications requiring a differential or single-ended output configuration should size R_{LOAD} accordingly. Refer to Applying the AD9772A Output Configurations section for examples of various output configurations.

The most significant improvement in the AD9772A's distortion and noise performance is realized using a differential output configuration. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be substantially reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the reconstructed waveform's frequency content increases and/or its amplitude decreases. The distortion and noise performance of the AD9772A is also dependent on the full-scale current setting, I_{OUTFS}. Although I_{OUTFS} can be set between 2 mA and 20 mA, selecting an I_{OUTFS} of 20 mA will provide the best distortion and noise performance.

In summary, the AD9772A achieves the optimum distortion and noise performance under the following conditions:

1. Positive voltage swing at I_{OUTA} and I_{OUTB} limited to 0.5 V.
2. Differential operation.
3. I_{OUTFS} set to 20 mA.
4. PLL clock multiplier disabled.

Note that the majority of the ac characterization curves for the AD9772A are performed under the above-mentioned operating conditions.

DIGITAL INPUTS/OUTPUTS

The AD9772A consists of several digital input pins used for data, clock, and control purposes. It also contains a single digital output pin, PLLLOCK, which is used to monitor the status of the internal PLL clock multiplier or provide a 1× clock output. The 14-bit parallel data inputs follow standard positive binary coding, where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch and is designed to support an input data rate as high as 160 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth as shown in Figures 1a and 1b. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met. The digital inputs (excluding CLK+ and CLK–) are CMOS compatible with its logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (i.e., DVDD or CLKVDD) or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

The internal digital circuitry of the AD9772A is capable of operating over a digital supply range of 3.1 V to 3.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers $V_{OH(MAX)}$. Although a DVDD of 3.3 V will typically ensure proper compatibility with most TTL logic families, series 200 Ω resistors are recommended between the TTL logic driver and digital inputs to limit the peak current through the ESD protection diodes if $V_{OH(MAX)}$ exceeds DVDD by more than 300 mV. Figure 19 shows the equivalent digital input circuit for the data and control inputs.

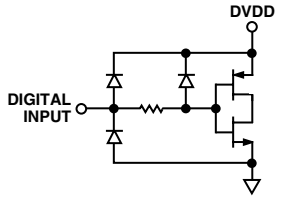


Figure 19. Equivalent Digital Input

The AD9772A features a flexible differential clock input operating from separate supplies (i.e., CLKVDD, CLKCOM) to achieve optimum jitter performance. The two clock inputs, CLK+ and CLK–, can be driven from a single-ended or differential clock source. For single-ended operation, CLK+ should be driven by a single-ended logic source while CLK– should be set to the logic source's threshold voltage via a resistor divider/capacitor network referenced to CLKVDD as shown in Figure 20. For differential operation, both CLK+ and CLK– should be biased to CLKVDD/2 via a resistor divider network as shown in Figure 21. An RF transformer as shown in Figure 3 can also be used to convert a single-ended clock input to a differential clock input.

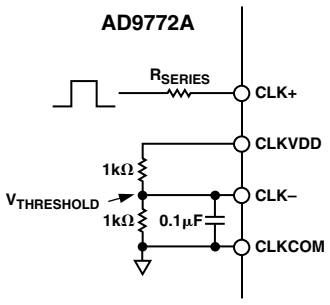


Figure 20. Single-Ended Clock Interface

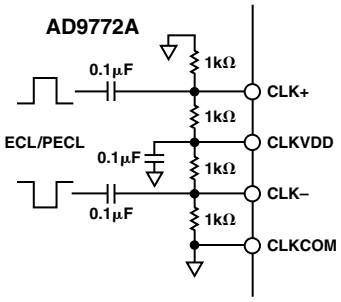


Figure 21. Differential Clock Interface

The quality of the clock and data input signals are important in achieving the optimum performance. The external clock driver circuitry should provide the AD9772A with a low jitter clock input, which meets the min/max logic levels while providing fast edges. Although fast clock edges help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform, the high gain-bandwidth product of the AD9772A's differential comparator can tolerate sine wave inputs as low as 0.5 V p-p, with minimal degradation in its output noise floor.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 50 Ω to 200 Ω) between the AD9772A digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough.

SLEEP MODE OPERATION

The AD9772A has a SLEEP function that turns off the output current and reduces the analog supply current to less than 6 mA over the specified supply range of 3.1 V to 3.5 V. This mode can be activated by applying a Logic Level 1 to the SLEEP pin. The AD9772A takes less than 50 ns to power down and approximately 15 µs to power back up.

POWER DISSIPATION

The power dissipation, P_D, of the AD9772A is dependent on several factors, including

1. AVDD, PLLVDD, CLKVDD, and DVDD, the power supply voltages.
2. I_{OUTFS}, the full-scale current output.
3. f_{DATA}, the update rate.
4. The reconstructed digital input waveform.

The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, and is not sensitive to f_{DATA}.

Conversely, I_{DVDD} is dependent on both the digital input waveform and f_{DATA}. Figure 22 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{DATA}) for various update rates with DVDD = 3 V. The supply current from CLKVDD and PLLVDD is relatively insensitive to the digital input waveform, but directly proportional to the update rate as shown in Figure 23.

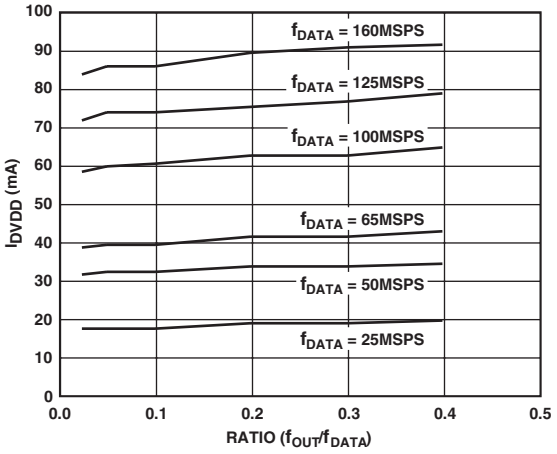


Figure 22. I_{DVDD} vs. Ratio @ DVDD = 3.3 V

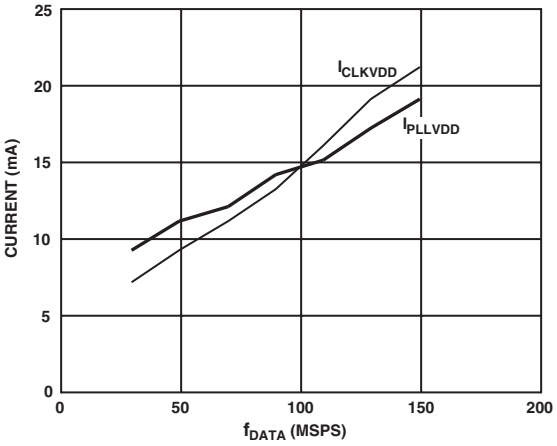


Figure 23. I_{PLLVDD} and I_{CLKVDD} vs. f_{DATA}

APPLYING THE AD9772A OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9772A. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA for optimum performance. For applications requiring the optimum dynamic performance, a differential output configuration is highly recommended. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level-shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 24. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's pass band. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only and its linearity performance degrades at the low end of its frequency range due to core saturation.

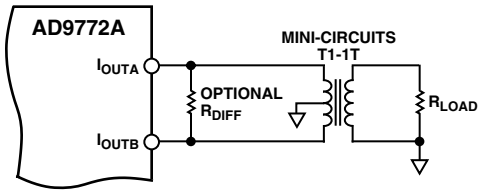


Figure 24. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9772A. A differential resistor, R_{DIFF}, may be inserted into applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR (Voltage Standing Wave Ratio). Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 25. The AD9772A is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DAC's high slewing output from overloading the op amp's input.

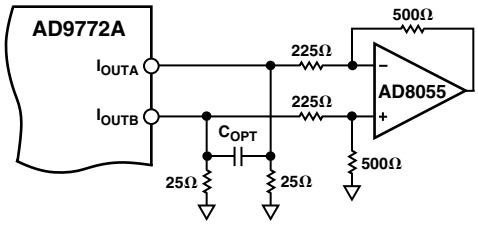


Figure 25. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8055 is configured to provide some additional signal gain. The op amp must operate from a dual supply since its output is approximately ±1.0 V. A high speed amplifier, capable of preserving the differential performance of the AD9772A while meeting other system level objectives (i.e., cost, power), should be selected. The op amp's differential gain, gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 26 provides the necessary level shifting required in a single-supply system. In this case, AVDD, the positive analog supply for both the AD9772A and the op amp, is also used to level-shift the differential output of the AD9772A to midsupply (i.e., AVDD/2). The AD8057 is a suitable op amp for this application.

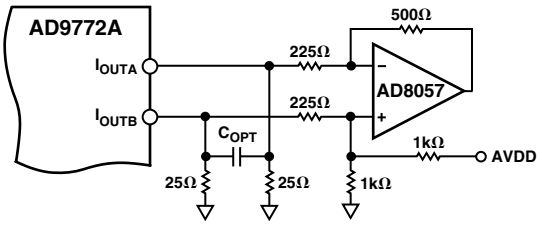


Figure 26. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 27 shows the AD9772A configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA}. The unused output (I_{OUTB}) should be connected to ACOM directly. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Outputs section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

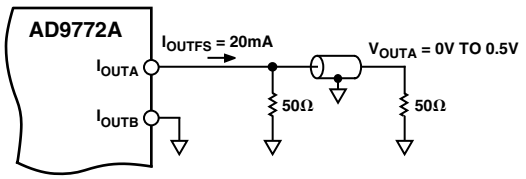


Figure 27. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED BUFFERED VOLTAGE OUTPUT

Figure 28 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9772A output current. U1 maintains I_{OUTA} (or I_{OUTB}) at virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates is often limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage, and its full-scale output voltage is simply the product of

RFB and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

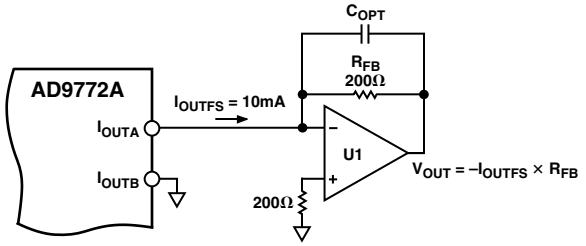


Figure 28. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

The AD9772A contains the following five power supply inputs: AVDD, DVDD1, DVDD2, CLKVDD, and PLLVDD. The AD9772A is specified to operate over a 3.1 V to 3.5 V supply range, thus accommodating a 3.3 V power supply with up to ±6% regulation. However, the following two conditions must be adhered to when selecting power supply sources for AVDD, DVDD1–DVDD2, CLKVDD, and PLLVDD:

1. PLLVDD = CLKVDD = 3.1 V–3.5 V when PLL clock multiplier enabled. (Otherwise PLLVDD = PLLCOM)
2. DVDD1–DVDD2 = CLKVDD ± 0.30 V

To meet the first condition, PLLVDD must be driven by the same power source as CLKVDD with each supply input independently decoupled with a 0.1 µF capacitor to its respective grounds. To meet the second condition, CLKVDD can share the power supply source as DVDD1–DVDD2, using the decoupling network shown in Figure 29 to isolate digital noise from the sensitive CLKVDD (and PLLVDD) supply. Alternatively, separate precision voltage regulators can be used to ensure that condition two is met.

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing, and supply bypassing and grounding. Figures 37 to 44 illustrate the recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9772A evaluation board.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9772A features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. AVDD, CLKVDD, and PLLVDD must be powered from a clean analog supply and decoupled to their respective analog common (i.e., ACOM, CLKCOM, and PLLCOM) as close to the chip as physically possible. Similarly, DVDD1 and DVDD2, the digital supplies, should be decoupled to DCOM.

For those applications requiring a single 3.3 V supply for both the analog, digital, and phase-lock loop supply, a clean AVDD and/or CLKVD may be generated using the circuit shown in Figure 29. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR-type electrolytic and tantalum capacitors.

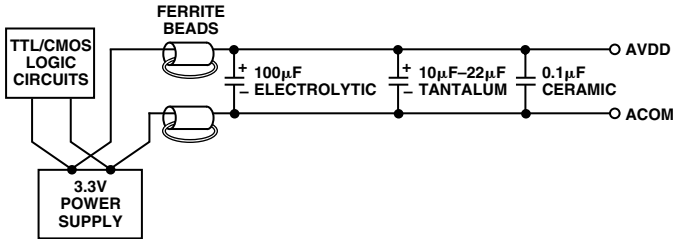


Figure 29. Differential LC Filter for 3.3 V

Maintaining low noise on power supplies and ground is critical to obtain optimum results from the AD9772A. If properly implemented, ground planes can perform a host of functions on high speed circuit boards, such as bypassing and shielding current transport. In mixed-signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference, and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC. On the analog side, this includes the DAC output signal, reference signal, and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some free capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct, and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistors should be considered. The necessity and value of these resistors will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' Application Note AN-333.

APPLICATIONS
MULTICARRIER

The AD9772A's wide dynamic range performance makes it well suited for next generation base station applications in which it reconstructs multiple modulated carriers over a designated frequency band. Cellular multicarrier and multimode radios are often referred to as software radios since the carrier tuning and modulation scheme is software programmable and performed digitally. The AD9772A is the recommended TxDAC in Analog Device SoftCell chipset, which comprises the AD6622, Quadrature Digital Upconverter IC, along with its companion Rx Digital Downconverter IC, the AD6624, and 14-bit, 65 MSPS ADC, the AD6644. Figure 30 shows a generic software radio Tx signal chain based on the AD9772A/AD6622.

Figure 31 shows a spectral plot of the AD9772A operating at 64.54 MSPS, reconstructing eight IS-136 modulated carriers spread over a 25 MHz band. For this particular test scenario, the AD9772A exhibited 74 dBc SFDR performance along with a carrier-to-noise ratio (CNR) of 73 dB. Figure 32 shows a spectral plot of the AD9772A operating at 52 MSPS, reconstructing four equal GSM carriers spread over a 15 MHz band. The SFDR and CNR (in 100 kHz BW) measured to be 76 dBc and 83.4 dB, respectively, along with a channel power of –13.5 dBFS. Note, the test vectors were generated using Rohde & Schwarz's WinIQSIM software.

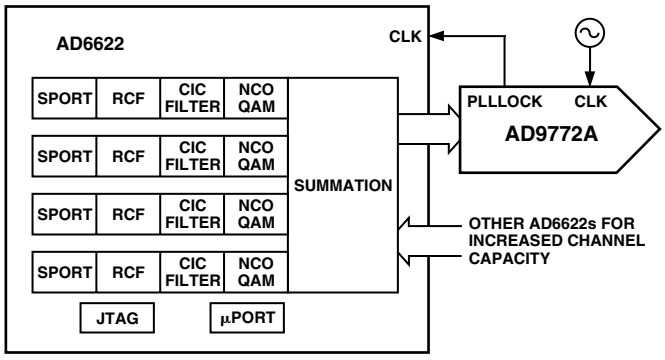


Figure 30. Generic Multicarrier Signal Chain Using the AD6622 and AD9772A

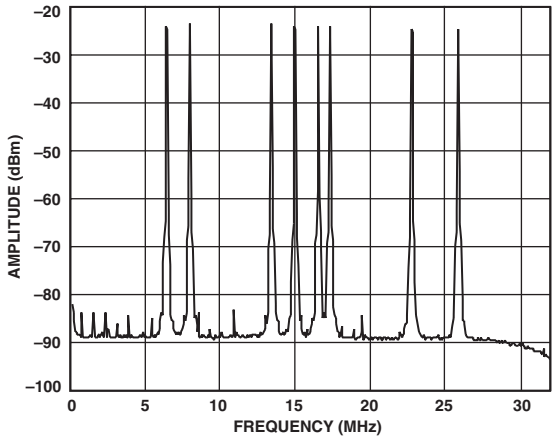


Figure 31. Spectral Plot of AD9772A Reconstructing Eight IS-136 Modulated Carriers @ f_{DATA} = 64.54 MSPS, PLLVDD = 0

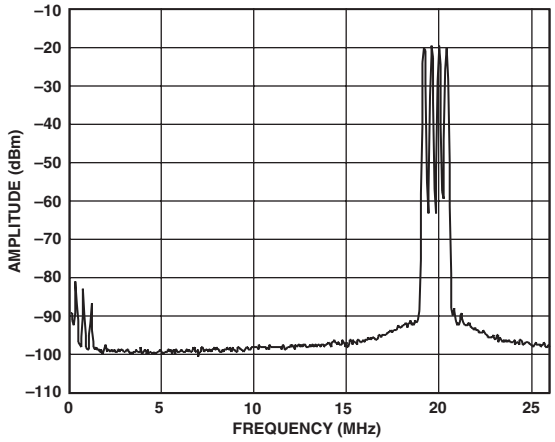


Figure 32. Spectral Plot of AD9772A Reconstructing Four GSM Modulated Carriers @ f_{DATA} = 52 MSPS, PLLVDD = 0

Although the above IS-136 and GSM spectral plots are representative of the AD9772A's performance for a particular set of test conditions, the following recommendations are offered to maximize the performance and system integration of the AD9772A into multicarrier applications:

1. To achieve the highest possible CNR, the PLL clock multiplier should be disabled (i.e., PLLVDD to PLLCOM) and the AD9772A's clock input driven with a low jitter/phase noise clock source at twice the input data rate. In this case, the divide-by-two clock appearing at PLLLOCK should serve as the master clock for the digital upconverter IC(s) such as the AD6622. PLLLOCK should be limited to a fanout of one.
2. The AD9772A achieves its optimum noise and distortion performance when configured for baseband operation along with a differential output and a full-scale current, I_{OUTFS}, set to approximately 20 mA.
3. Although the 2× interpolation filters frequency roll-off provides a maximum reconstruction bandwidth of $0.422 \times f_{DATA}$, the optimum adjacent image rejection (due to the interpolation process) is achieved (i.e., > 73 dBc) if the maximum channel assignment is kept below $0.400 \times f_{DATA}$.
4. To simplify the subsequent IF stages filter requirements (i.e., mixer image and LO rejection), it is often advantageous to offset the frequency band from dc to relax the transition band requirements of the IF filter.
5. Oversampling the frequency band often results in improved SFDR and CNR performance. This implies that the data input rate to the AD9772A is greater than $f_{PASSBAND}/0.4$ where $f_{PASSBAND}$ is the maximum bandwidth in which the AD9772A will be required to reconstruct and place carriers. The improved noise performance results in a reduction in the TxDAC's noise spectral density due to the added process gain realized with oversampling. Also, higher oversampling ratios provide greater flexibility in the frequency planning.

BASEBAND SINGLE-CARRIER

The AD9772A is also well suited for wideband single-carrier applications such as WCDMA and multilevel QAM whose modulation scheme requires wide dynamic range from the reconstruction DAC to achieve the out-of-band spectral mask as well as the in-band CNR performance. Many of these applications strategically place the carrier frequency at one quarter of the DAC's input data rate (i.e., $f_{DATA}/4$) to simplify the digital modulator design. Since this constitutes the first fixed IF frequency, the frequency tuning is accomplished at a later IF stage. To enhance the modulation accuracy as well as reduce the shape factor of the second IF SAW filter, many applications will often specify the pass band of the IF SAW filter to be greater than the channel bandwidth. The trade-off is that the TxDAC must now meet the particular application's spectral mask requirements within the extended pass band of the second IF, which may include two or more adjacent channels.

Figure 33 shows a spectral plot of the AD9772A reconstructing a test vector similar to those encountered in WCDMA applications with the following exception. WCDMA applications prescribe a root raised cosine filter with an alpha = 0.22, which limits the theoretical ACPR of the TxDAC to about 70 dB. This particular test vector represents white noise that has been band-limited by a brick wall band-pass filter with the same pass band such that its maximum ACPR performance is theoretically 83 dB and its peak-to-rms ratio is 12.4 dB. As Figure 33 reveals, the AD9772A is capable of approximately 78 dB ACPR performance when one accounts for the additive noise/distortion contributed by the FSEA30 spectrum analyzer.

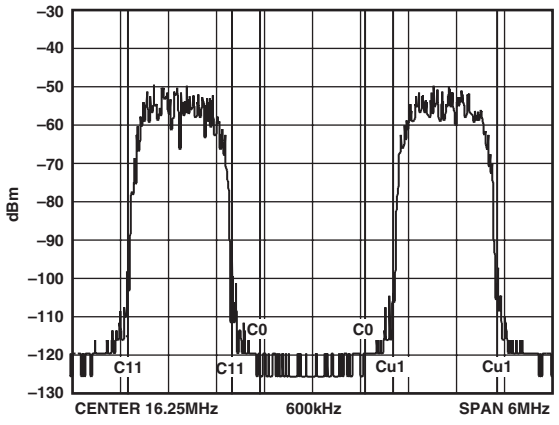


Figure 33. AD9772A Achieves 78 dB ACPR Performance Reconstructing a WCDMA-Like Test Vector with f_{DATA} = 65.536 MSPS and PLLVDD = 0

DIRECT IF

As discussed in the Digital Modes of Operation section, the AD9772A can be configured to transform digital data representing baseband signals into IF signals appearing at odd multiples of the input data rate (i.e., $N \times f_{DATA}$ where N = 1, 3, . . .). This is accomplished by configuring the MOD1 and MOD0 digital inputs high. Note, the maximum DAC update rate of 400 MSPS limits the data input rate in this mode to 100 MSPS when the zero-stuffing operation is enabled (i.e., MOD1 high). Applications requiring higher IFs (i.e., 140 MHz) using higher data rates should disable the zeros-stuffing operation. Also, to minimize the effects of the PLL clock multipliers phase noise as shown in Figure 9, an external low jitter/phase noise clock source equal to $4\times f_{DATA}$ is recommended.

Figure 34 shows the actual output spectrum of the AD9772A reconstructing a 16-QAM test vector with a symbol rate of 5 MSPS. The particular test vector was centered at $f_{DATA}/4$ with f_{DATA} = 100 MSPS, and f_{DAC} = 400 MHz. For many applications, the pair of images appearing around f_{DATA} will be more attractive since they have the flattest pass band and highest signal power. Higher images can also be used with the understanding that these images will have reduced pass-band flatness, dynamic range, and signal power, thus reducing the CNR and ACP performance. Figure 35 shows a dual-tone SFDR amplitude sweep at the various IF images with f_{DATA} = 100 MSPS and f_{DAC} = 400 MHz and the two tones centered around $f_{DATA}/4$. Note, since an IF filter is assumed to precede the AD9772A, the SFDR was measured over a 25 MHz window around the images occurring at 75 MHz, 125 MHz, 275 MHz, and 325 MHz.

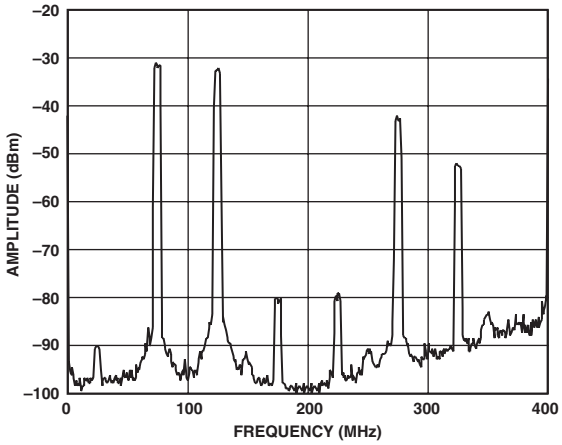


Figure 34. Spectral Plot of 16-QAM Signal in Direct IF Mode at f_{DATA} = 100 MSPS

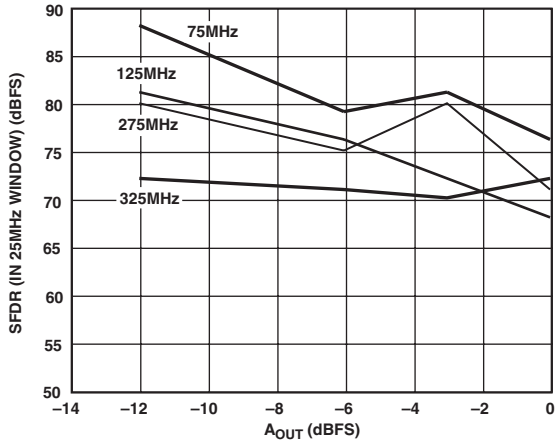


Figure 35. Dual-Tone Windowed SFDR vs. A_{OUT} @ f_{DATA} = 100 MSPS

Regardless of which image is selected for a given application, the adjacent images must be sufficiently filtered. In most cases, a SAW filter providing differential inputs represents the optimum device for this purpose. For single-ended SAW filters, a balanced-to-unbalanced RF transformer is recommended. The AD9772A's high output impedance provides a certain amount of flexibility in selecting the optimum resistive load, R_{LOAD}, as well as any matching network.

For many applications, the data update rate to the DAC (i.e., f_{DATA}) must be some fixed integer multiple of some system reference clock (i.e., GSM – 13 MHz). Furthermore, these applications prefer to use standard IF frequencies which offer a large selection of SAW filter choices of varying passbands (i.e., 70 MHz). These applications may still benefit from the AD9772A's direct IF mode capabilities when used in conjunction with a digital upconverter such as the AD6622. Since the AD6622 can digitally synthesize and tune up to four modulated carriers, it is possible to judiciously tune these carriers in a region which may fall within an IF filter's pass band upon reconstruction by the AD9772A. Figure 36 shows an example in which four carriers were tuned around 18 MHz with a digital upconverter operating at 52 MSPS such that when reconstructed by the AD9772A in the IF mode, these carriers fall around a 70 MHz IF.

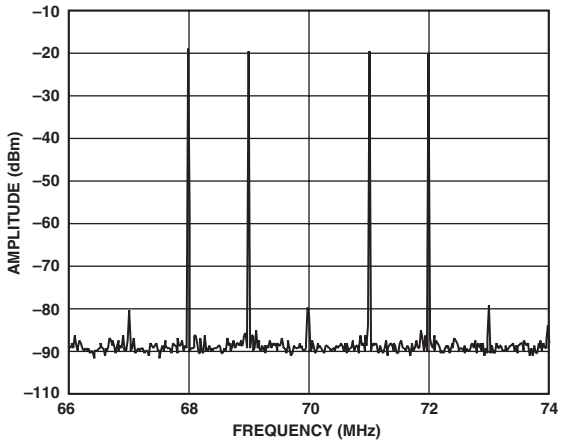


Figure 36. Spectral Plot of Four Carriers at 60 MHz IF with f_{DATA} = 52 MSPS, PLLVDD = 0

AD9772A EVALUATION BOARD

The AD9772-EB is an evaluation board for the AD9772A TxDAC. Careful attention to layout and circuit design, combined with prototyping area, allows the user to easily and effectively evaluate the AD9772A in different modes of operation.

Referring to Figures 37 and 38, the AD9772A's performance can be evaluated differentially or single-endedly using a transformer, differential amplifier, or directly coupled output. To evaluate the output differentially using the transformer, remove jumpers JP12 and JP13 and monitor the output at J6 (IOUT). To evaluate the output differentially, remove the transformer (T2) and install jumpers JP12 and JP13. The output of the amplifier can be evaluated at J13 (AMPOUT). To evaluate the AD9772A single-endedly and directly coupled, remove the transformer and jumpers (JP12 and JP13), and install resistors R16 or R17 with 0 Ω.

The digital data to the AD9772A comes across a ribbon cable which interfaces to a 40-pin IDC connector. Proper termination or voltage scaling can be accomplished by installing RN2 and/or RN3 SIP resistor networks. The 22 Ω DIP resistor network, RN1, must be installed and helps reduce the digital data edge rates. A single-ended CLOCK input can be supplied via the ribbon cable by installing JP8 or more preferably via the SMA connector, J3 (CLOCK). If the CLOCK is supplied by J3, the AD9772A can be configured for a differential clock interface by installing jumpers JP1 and configuring JP2, JP3, and JP9 for the DF position. To configure the AD9772A clock input for a single-ended clock interface, remove JP1 and configure JP2, JP3, and JP9 for the SE position.

The AD9772A's PLL clock multiplier can be disabled by configuring jumper JP5 for the L position. In this case, the user must supply a clock input at twice (2×) the data rate via J3 (CLOCK). The 1× clock is made available on SMA connector J1 (PLLLOCK), and should be used to trigger a pattern generator directly or via a programmable pulse generator. Note that PLLLOCK is capable of providing a 0 V to 0.85 V output into a 50 Ω load. To enable the PLL clock multiplier, JP5 must be configured for the H position. In this case, the clock may be supplied via the ribbon cable (i.e., JP8 installed) or J3 (CLOCK). The divide-by-N ratio can be set by configuring JP6 (DIV0) and JP7 (DIV1).

The AD9772A can be configured for baseband or direct IF mode operation by configuring jumpers JP11 (MOD0) and JP10 (MOD1). For baseband operation, JP10 and JP11 should be configured in the L position. For direct IF operation, JP10 and JP11 should be configured in the H position. For direct IF operation without zero-stuffing, JP11 should be configured in the H position while JP10 should be configured in the low position.

The AD9772A's voltage reference can be enabled or disabled via JP4 (EXT REF IN). To enable the reference, configure JP in the INT position. A voltage of approximately 1.2 V will appear at the TP6 (REFIO) test point. To disable the internal reference, configure JP4 in the EXT position and drive TP6 with an external voltage reference. Lastly, the AD9772A can be placed in the SLEEP mode by driving the TP11 test point with logic level high input signal.

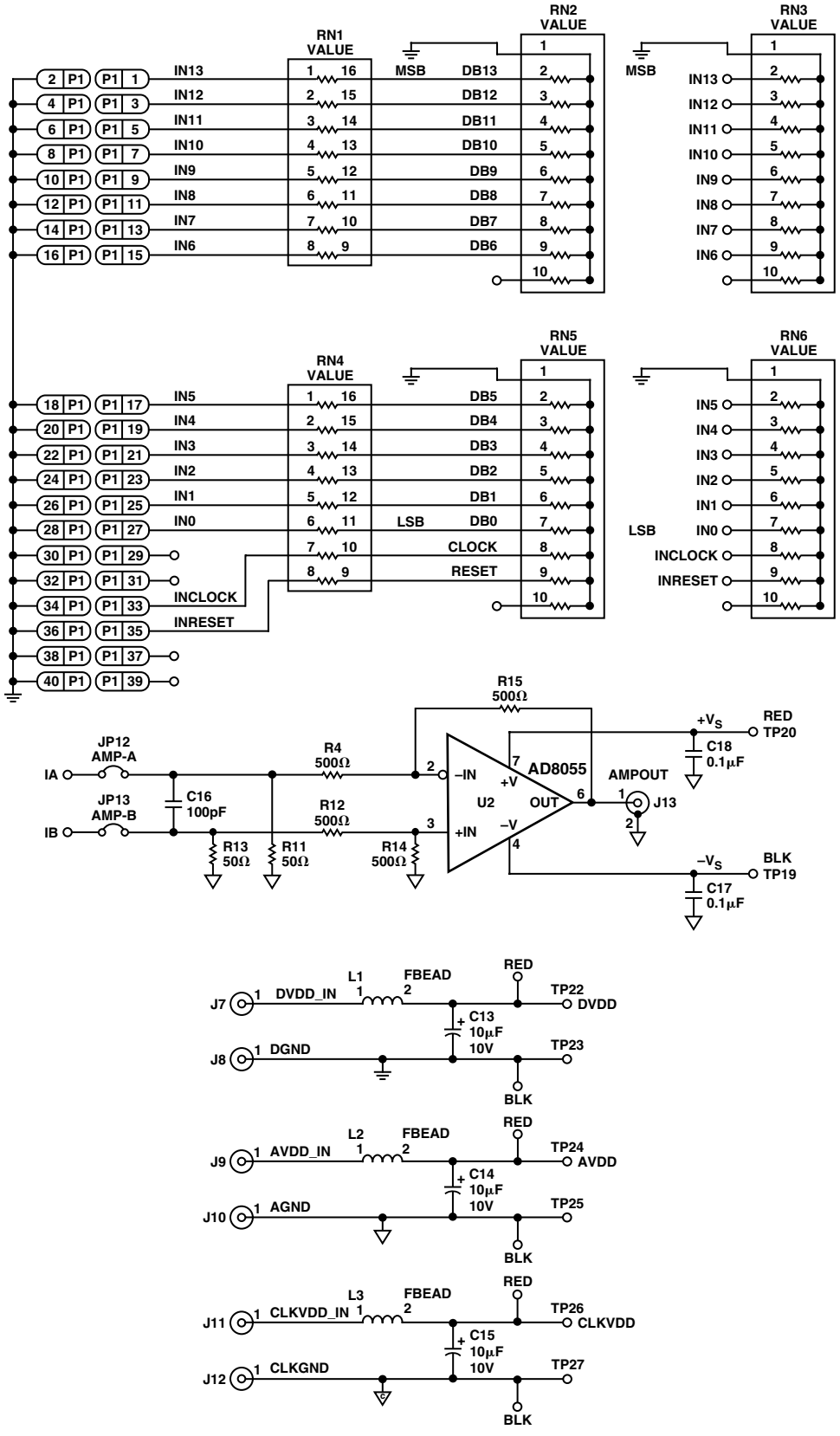


Figure 37. Drafting Schematic of Evaluation Board

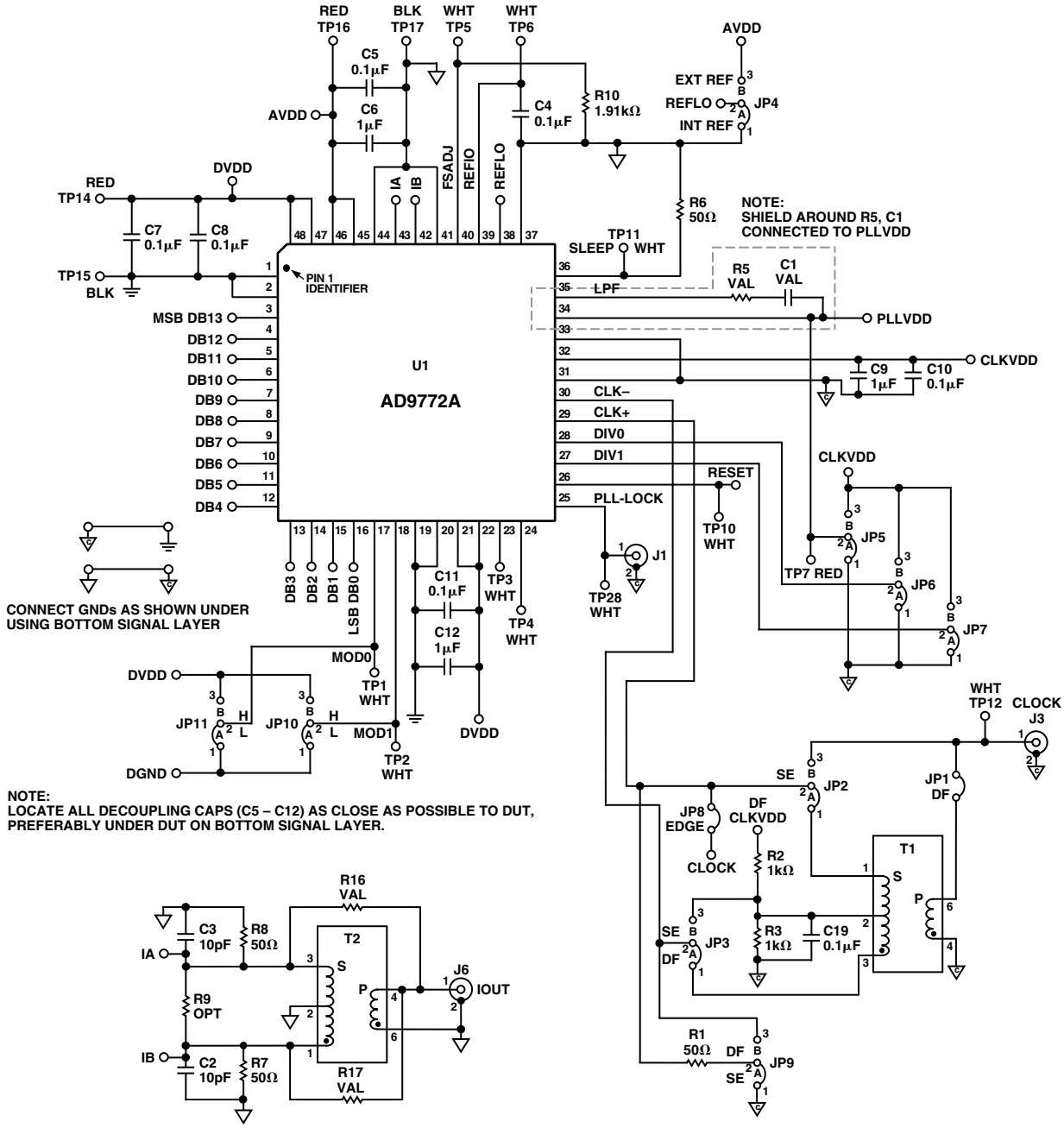


Figure 38. Drafting Schematic of Evaluation Board (continued)

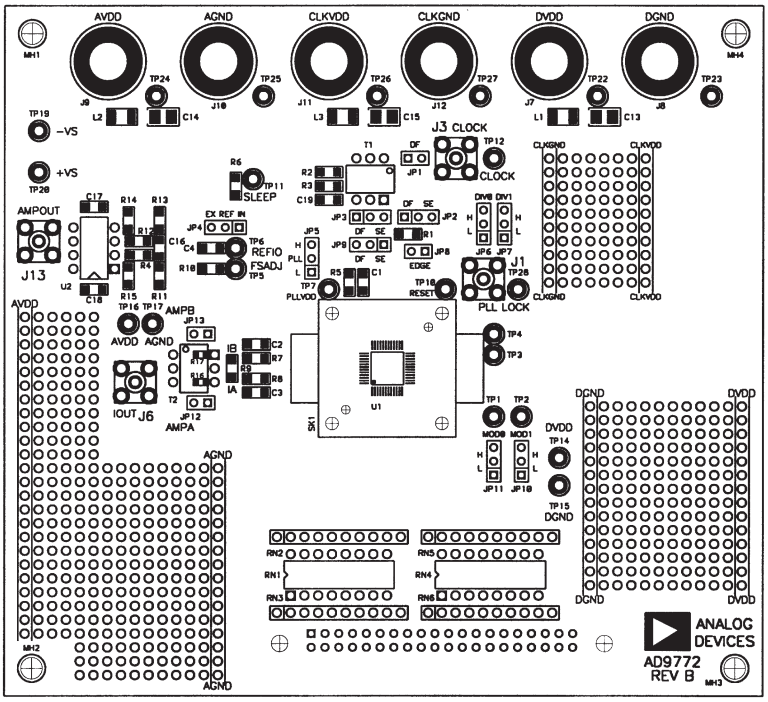


Figure 39. Silkscreen Layer—Top

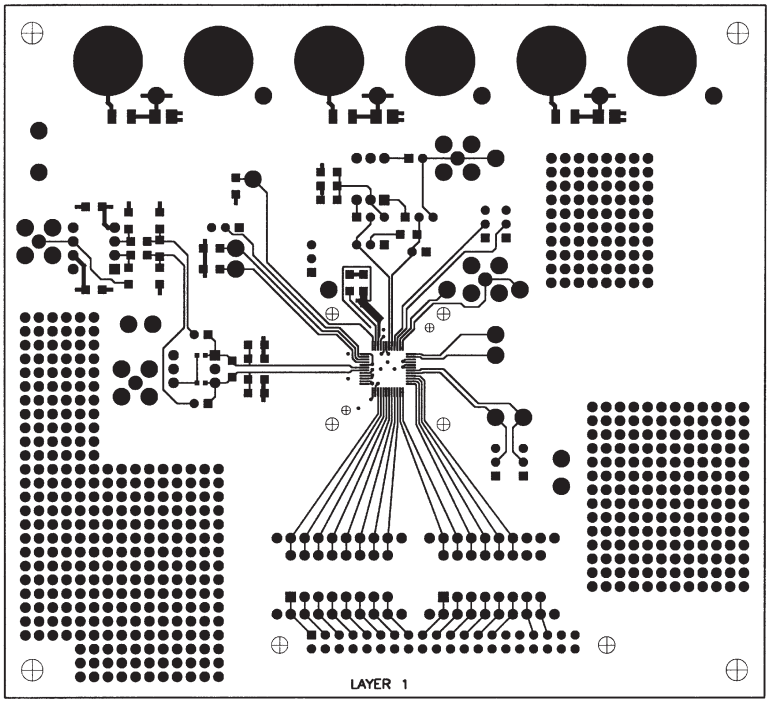


Figure 40. Component Side PCB Layout (Layer 1)

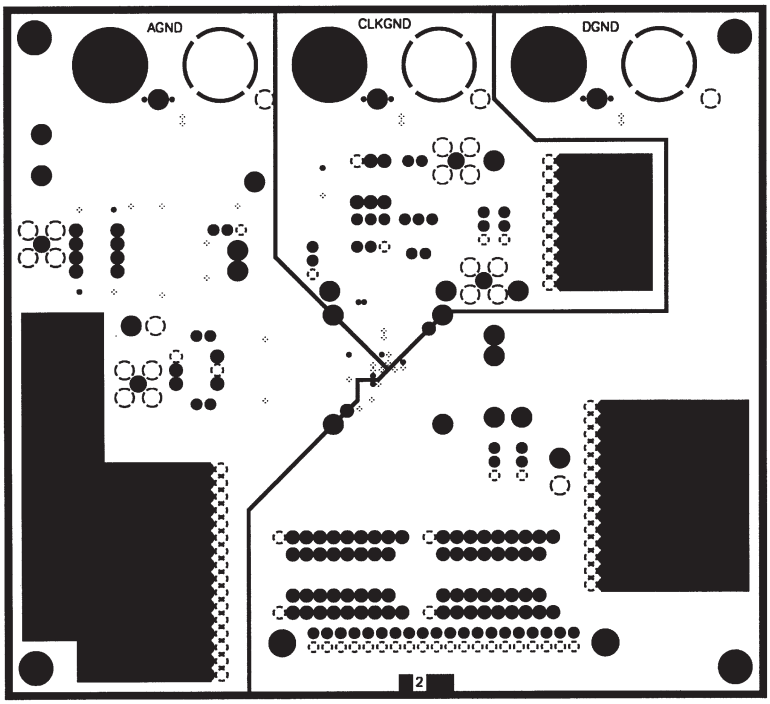


Figure 41. Ground Plane PCB Layout (Layer 2)

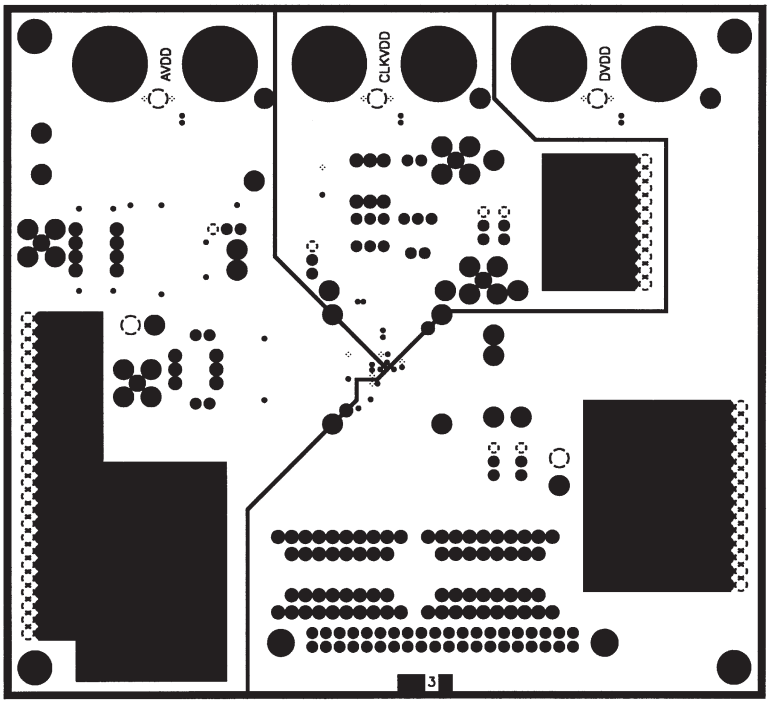


Figure 42. Power Plane PCB Layout (Layer 3)

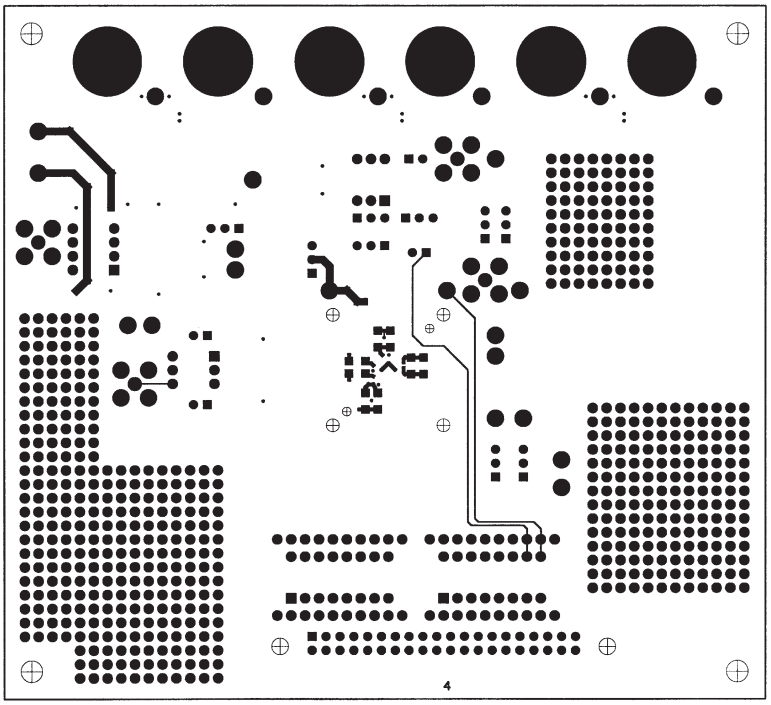


Figure 43. Solder Side PCB Layout (Layer 4)

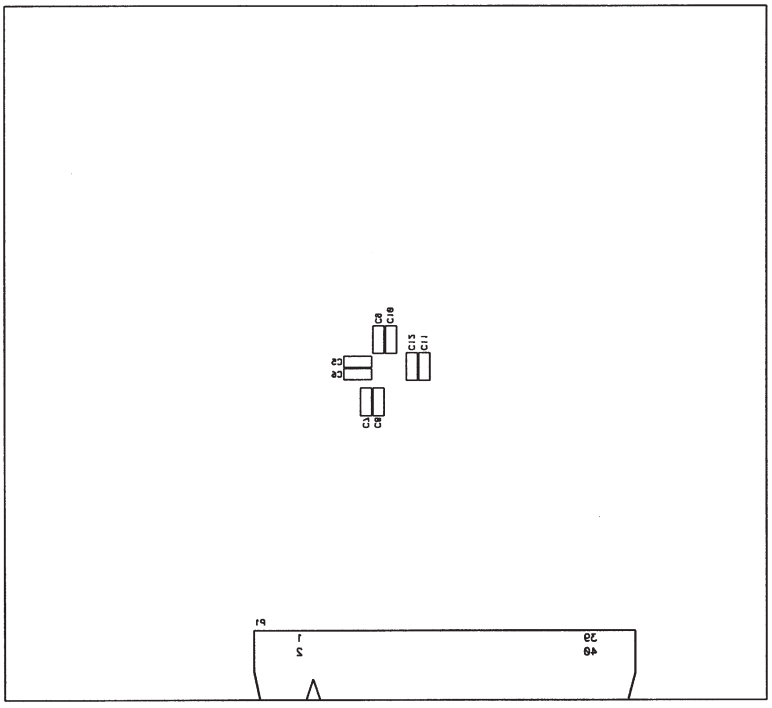
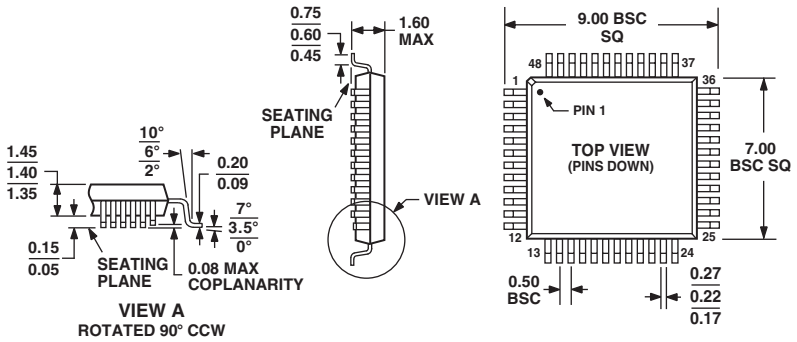


Figure 44. Silkscreen Layer—Bottom

OUTLINE DIMENSIONS

48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Revision History

Location	Page
6/03—Data Sheet changed from REV. A to REV. B.	
Change to FEATURES	1
Change to DC SPECIFICATIONS	2
Change to DIGITAL FILTER SPECIFICATIONS	5
ORERING GUIDE Updated	6
Change to PIN FUNCTION DESCRIPTIONS	7
Change to Figure 13a and 13b	15
Change to DIGITAL INPUTS/OUTPUTS	18
Change to SLEEP MODE OPERATION	19
Change to Figure 22	19
Change to Figure 23	19
Change to POWER AND GROUND CONSIDERATIONS	21
Change to Figure 29	21
Update to OUTLINE DIMENSIONS	30
3/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to DIGITAL SPECIFICATION	4
Edits to ABSOLUTE MAXIMUM RATINGS	6
Change to TPC 11	10
Change to Figure 9 Caption	14
Change to Figure 13a and 13b	15